

**KS10
Maintenance
Guide
Volume I**

First Edition, June 1979

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	VMS	IAS

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To the Reader:

CONFIDENTIALITY - This guide contains Company Confidential information and is intended for use by DIGITAL field engineers only. Refer to the Field Service Methods and Procedures Manual for DIGITAL policy pertaining to handling confidential information.

OBJECTIVE - The objective of this guide is to organize and present that information which is most used during KS10 maintenance activities. This document is directed toward qualified KS10-trained technical personnel.

To maintain accuracy and improve this guide in subsequent revisions, we need feedback. Please forward any information or suggestions that would increase the usefulness of the guide to:

LCG Tools Supervisor
MR1-1 S35

RELATED KS10 DOCUMENTS

KS10-Based DECSYSTEM-2020 Technical Manual, EK-0KS10-TM-002

KS10-Based DECSYSTEM-2020 Installation Manual, EK-0KS10-IN-001

ORGANIZATION - The guide is divided into six sections.

1. **GENERAL INFORMATION** consists of miscellaneous maintenance information which cannot be classified and filed in any of the remaining four hardware sections.
2. **SWITCHES/JUMPERS** contains information pertaining to hardware switch positions and jumper connections.
3. **TABLES/MAPS** describes the process tables and bit maps associated with the KS10 mainframe and peripheral equipment.
4. **CHECKS/ADJUSTMENTS** consists of check and adjustment procedures performed during preventive and corrective maintenance.
5. **DIAGRAMS/MULS** contains power supply layouts and module utilization lists associated with KS10-based systems.
6. **SOFTWARE** contains standard boot procedure, pre-boot error messages, diagnostic program hierarchies, standard console messages, console commands, and console error messages.

The information in each hardware section is indexed and arranged according to unit and subsystem (i.e., CPU, memory, disk, tape, and I/O).

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GEN. INFO.

NOTES

TELEPHONE NUMBERS

Digital Diagnostic Center (10/20/ 11/70, and VAX)

NORAM Colorado Springs, Colorado

800-525-6570 Use this number to log a service call for DDC response.

303-599-4000 Use this number to contact specific DDC engineers. This number should also be used by Canada to contact DDC.

Software Hot Line (10/20 only)

617-481-9511 Extension 6492 Marlboro, Massachusetts

Diagnostic Hot Line (10/20 only)

617-481-9511 Extension 6556 Marlboro, Massachusetts

Technical Assistance Centers

Corporate (10/20 only)

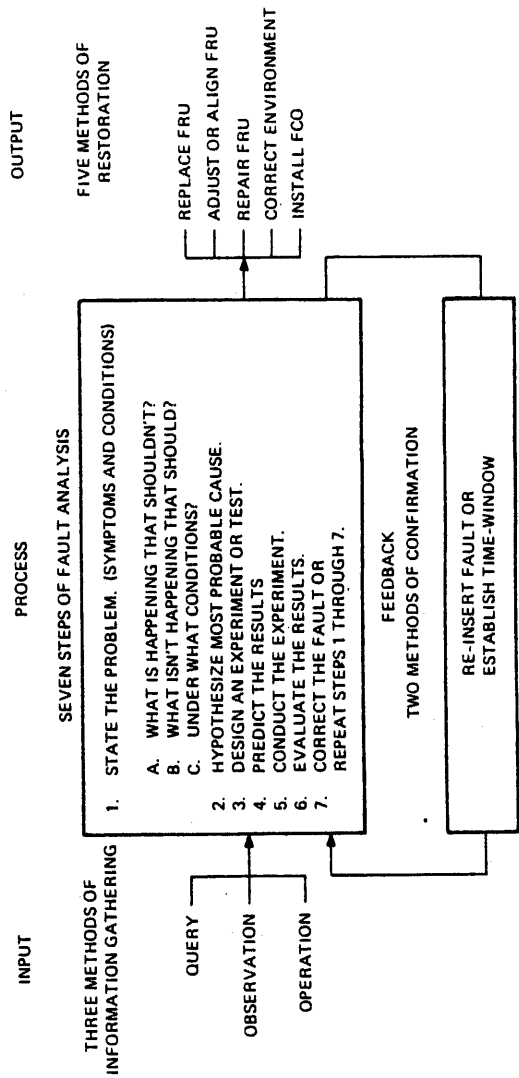
617-481-9511 Extension 6903 or 6904 Marlboro, Massachusetts

Corporate (non-10/20)

617-897-5111 Extension 5901 Maynard, Massachusetts

Region

District



MR 2502

GEN. INFO.

Module Configuration Information

1. M7819 (DZ11) (Lowest Acceptable CS Rev E) - A fully configured KS10-System will have up to four M7819 (DZ11) modules. Their address and vector assignments will be according to the following chart.
2. M7867 (DUP11-DA) (Lowest acceptable CS Rev F) - A fully configured KS10 subsystem will have up to two M7867 (DUP11-DA) modules. Their address and vector assignments will be according to the following chart.
3. M8204 (KMC11) (Lowest acceptable CS Rev D) - A fully configured KS10 system will have one M8204 (KMC11) module. Its address and vector assignments will be according to the following chart.

Address and Vector Table

Device	#	Address	Vector	Unit	BR Level
RH11	1	776700	254	1	6
	2	772440	224	3	6
LP20	1	775400	754	3	4
	2	775420	750	3	4
DZ11	1	760010	340	3	5
	2	760020	350	3	5
	3	760030	360	3	5
	4	760040	370	3	5
KMC11	1	760540	540	3	5
	2	760550	550	3	5
DUP11	1	760300	570	3	5
	2	760310	600	3	5
CD11	1	777160	230	3	4

UNIBUS PIN ASSIGNMENTS
(BY PIN NUMBERS)

AA1 INIT L
 AA2 POWER (+5 V)
 AB1 INTR L
 AB2 GROUND
 AC1 DOO L
 AC2 GROUND
 AD1 DO2 L
 AD2 DO1 L
 AE1 DO4 L
 AE2 DO3 L
 AF1 DO6 L
 AF2 DO5 L
 AH1 DO8 L
 AH2 DO7 L
 AJ1 D10 L
 AJ2 DO9 L
 AK1 D12 L
 AK2 D11 L
 AL1 D14 L
 AL2 D13 L
 AM1 PA L (D16 L)
 AM2 D15 L
 AN1 GROUND
 AN2 PB L (D17 L)
 AP1 GROUND
 AP2 BBSY L
 AR1 GROUND
 AR2 SACK L
 AS1 GROUND
 AS2 NPR L
 AT1 GROUND
 AT2 BR 7 L
 AU1 NPG H
 AU2 BR 6 L
 AV1 BG 7 H
 AV2 GROUND
 BA1 BG6 H
 BA2 POWER (+5 V)
 BB1 BG 5 H
 BB2 GROUND
 BC1 BR 5 L
 BC2 GROUND
 BD1 GROUND
 BD2 BR 4 L
 BE1 GROUND
 BE2 BG 4 H
 BF1 ACLO L
 BF2 DCLO L
 BH1 AO1 L
 BH2 AOO L
 BJ1 AO3 L
 BJ2 AO2 L
 BK1 AO5 L
 BK2 AO4 L
 BL1 AO7 L
 BL2 AO6 L
 BM1 AO9 L
 BM2 AOB L
 BN1 A11 L
 BN2 A10 L
 BP1 A13 L
 BP2 A12 L
 BR1 A15 L
 BR2 A14 L
 BS1 A17 L
 BS2 A16 L
 BT1 GROUND
 BT2 C1 L
 BU1 SSYN L
 BU2 CO L
 BV1 MSYN L
 BV2 GROUND

UNIBUS PIN ASSIGNMENTS
(BY SIGNAL NAME)

AOO L BH2
 AO1 L BH1
 AO2 L BJ2
 AO3 L BJ1
 AO4 L BK2
 AO5 L BK1
 AO6 L BL2
 AO7 L BL1
 AO8 L BM2
 AO9 L BM1
 A10 L BN2
 A11 L BN1
 A12 L BP2
 A13 L BP1
 A14 L BR2
 A15 L BR1
 A16 L BS2
 A17 L BS1
 ACLO L BF1
 BBSY L AP2
 BG4 H BE2
 BG5 H BB1
 BG6 H BA1
 BG7 H AV1
 BR4 L BD2
 BR5 L BC1
 BR6 L AU2
 BR7 L AT2
 CO L BU2
 C1 L BT2
 DOO L AC1
 DO1 L AD2
 DO2 L AD1
 DO3 L AE2
 DO4 L AE1
 DO5 L AF2
 DO6 L AF1
 DO7 L AH2
 DO8 L AH1
 DO9 L AJ2
 D10 L AJ1
 D11 L AK2
 D12 L AK1
 D13 L AL2
 D14 L AL1
 D15 L AM2
 GROUND AB2
 GROUND AC2
 GROUND AN1
 GROUND AP1
 GROUND AR1
 GROUND AS1
 GROUND AT1
 GROUND AV2
 GROUND BB2
 GROUND BC2
 GROUND BD1
 GROUND BE1
 GROUND BT1
 GROUND BV2
 INIT L AA1
 INTR L AB1
 MSYN L BV1
 NPG H AU1
 NPR L AS2
 PA L (D16 L) AM1
 PB L (D17 L) AN2
 +5 V* AA2
 +5 V* BA2
 SACK L AR2
 DCLO L BF2
 SSYN L BU1

NOTES

- +5 V is wired to these pins to supply power to the bus terminator only.
- +5 V should never be connected via the Unibus between system units.

GEN. INFO.

EC - COMMAND - BREAKDOWN

00	01	02	03	04	05	06	07	08	09	10	11
J FIELD											
00	01	02	03	04	05	06	07	08	09	10	11
12	13	14	15	16	17	18	19	20	21	22	23
TIME CONTROL	CALL	SKIP ENABLE	SPECIAL ENABLE	DISPATCH ENABLE							
24	25	26	27	28	29	30	31	32	33	34	35
CRA PAR	CRY PAR	MEM WRITE	DISPATCH SELECT	SPECIAL SELECT	SKIP SELECT						
36	37	38	39	40	41	42	43	44	45	46	47
MAGIC NUMBER											
06	07	08	09	10	11	12	13	14	15	16	17

48	49	50	51	52	53	54	55	56	57	58	59
RAM WRITE	MULTI SHIFT	PAR ENBL	PAR ENBL	DIV IDE	MULTI PREC	00	01	02	03	04	05
60	61	62	63	64	65	66	67	68	69	70	71
ALU FUNCTION	LEFT SRC	RIGHT SRC	00	01	02	03	04	05	06	07	08
4	2	1	4	2	1	4	2	1	4	2	1
72	73	74	75	76	77	78	79	80	81	82	83
D BUS SELECT	DPA ADDRESS	DPCLK ENBL	DPCLK ENBL	DPCLK ENBL	DPCLK ENBL	DPCLK ENBL	DPCLK ENBL	DPCLK ENBL	DPCLK ENBL	DPCLK ENBL	DPCLK ENBL
84	85	86	87	88	89	90	91	92	93	94	95
RAM ADDRESS	ALU DESTINATION	SC ENB	FE ENB	PAR CHK L	PAR CHK R	CRM PAR	MARK				
4	2	1	1	1	1	1	1	1	1	1	1

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DROM A <0:5>				DROM B <6:11>				DROM J <12:23>				DROM J <24:35>																											
N.U.	00	01	02	03	N.U.	00	01	02	03	N.U.	00	01	02	03	04	05	06	07	AC DISP	A-J	READ TEST	WRT TEST	COND FUNC	VMA EN	WRT TXXX	N.U.													
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35				
E114				E114				E114				E113				E113				E113				E113															
13				13				13				13				13				13				13				13											
DM1				DP1				DR1				DS1				DC1				BN1				SR1				DD1				BP1				D-1			

<p>OPERAND FETCH MODE</p> <p>0 = READ 1 = WRITE 2 = DREAL 3 = DBLAC 4 = SHIFT 5 = DSHIFT 6 = FPI 7 = FP 10 = RD-PF 11 = DFP 12 = 10T</p> <p>DOUBLE READ DOUBLE AC SIMPLE SHIFT DOUBLE SHIFT FLOATING POINT IMMEDIATE FLOATING POINT READ, THEN START PREFETCH DOUBLE FLOATING POINT CHECK FOR I/O LEGAL, THEN SAME AS A - J.</p>	<p>STORE MODE (NORMAL) <6:11> STORE AS:</p> <p>4 = SELF 5 = DELAC 6 = DELB 15 = AC 16 = MEMORY 17 = BOTH</p> <p>FLOATING POINT MODE <6:11></p> <p> = ROUND ROUNG THE RESULT = MODE SEPARATE ADD/SUB AND DIV/MUL, ETC.</p> <p>FLB <10:11> STORE RESULT AS: 1 = AC 2 = MEMORY 3 = BOTH</p>	<p>WHEN THE DROM J FIELD IS USED TO FORM THE CRAM ADDRESS THRU THE DISP 20 MIXER (CRAT), HARDWARE FORCES CRA ADR J00: J03 TO 14, THEREFORE THE DROM J DISPATCH ADDRESS IS CONSIDERED TO BE 1400 + DROM J, OR BETWEEN 1400 AND 1777.</p>	<p><24> = AC DISP</p> <p><25> = A - J</p> <p><26> = READ <27> = WRT TEST <28> = COND FUNC <29> = VMA EN <30> = WRITE <31> = TXXX</p> <p>DISPATCH ON AC FIELD (IR 06-12). CRA ADR J00-07 DROM J00-03 + 1400 OR'D WITH IMMEDIATE DISPATCH. (A READ DISPATCH) CRA ADR J00-07 DROM J00-03 + 1400 OR'D WITH CRA ADR J08-11 DROM J04-07 START A READ AT AREAD START A WRITE TEST AT AREAD START A MEMORY CYCLE ON B WRITE LOAD THE VMA ON AREAD START A WRITE ON AREAD USED WITH LOGICAL TESTING AND MODIFICATIONS (OP CODE 6XX)</p>
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FIELD
 SIGNAL
 WORD BIT
 ROM BIT
 ROM
 SLOT
 PIN
 DEFAULT

Dispatch Word Format

MR 2837

GEN. INFO.

NOTES

GEN. INFO.

FIELD	RAMFILE ADDRESS, DBUS, DBM <36:44>	PARITY GENERATION AND HALF WORD CONTROL <46:50>	SPEC <51:56>	FULL FIELD <51:56> (DPF1&5, DPM1&A)	DISPATCH <57:62>
SIGNAL	RAM ADR 04 02 01	DBUS SEL 2 1 4 2 1	ENABLE 40 20 10 4 2 1	DECODE = BITS (SPEC/CONSOLE) (CRA 2)	ENABLE 40 20 10 4 2 1
WORD BIT	DBUS SEL 36 37 38	CLKR GENL CHKL CLKR GENR CHKR 46 48 47 48 49 50	SELECT 54 65 56	WRITE PAGE TABLE DOING NICOND DISPATCH LOAD/PXCT FLAGS MEM WAIT	SELECT 57 58 59 60 61 62
GRAM BIT	DBUS SEL 84 85 86	CLKR GENL CHKL CLKR GENR CHKR 78 50 82 78 51 93	12	FORCE PREVIOUS CONTEXT LOAD XR = PXCT FIELD SELECTS AC BLOCK LOAD APN/AC/PC SET APN/AC/PC CLEAR PAGE FAULT CONDITION	SELECT 21 22 23 27 28 29
SLOT	ASZ B/J	11	12	20 PREV 21 LOADXR 22 APRFLGS 23 CLRBN 24 CLRPR 25 CLRPR1 27 MEMCLR	12
FN	A/J	D-1	12	23 APRFLGS 24 CLRBN 25 CLRPR 27 MEMCLR	BN1 CF1 CH1 BN2 CF2 CM1 R2 J2 R2
DEFAULT	D-4	D-1	D-00	34 SWEEP 38 PXCTOFF 40 INHCR/18 41 LOADIR 43 LDPI 44 ASHOV 45 EXACTY 46 EXACTY 47 BDACBLK 61 LDINST	D = 70
	(DPE#)	(DPM1&2)	SELECT FIELD <54:56>	34 SWEEP 38 PXCTOFF 40 INHCR/18 41 LOADIR 43 LDPI 44 ASHOV 45 EXACTY 46 EXACTY 47 BDACBLK 61 LDINST	(CRA1 DPE#) 00 CONSOLE CONSOLE DISP 12 DROM 13 AREAD 31 DPLEFT 34 NORMA 35 DP 36 ADISP 37 BDISP 41 RETURN 62 MUL 63 PAGE FAIL 64 NICOND 65 BYTE 66 EAMODE 67 SCAD 0 71 SCAD 71 SCAD 71 SCAD 71 SCAD
	0 AC# 1 AC#* 2 XR# 4 VMA 6 RAM 7 #	CLKL CLOCK LEFT 1/2 OF MACHINE GENL STORE PARITY 1/2 DBUS CHKL PARITY CLKR } SAME AS ABOVE BUT CHKR } RIGHT HALF "AD PARITY OK <108> 0=0	DP SELECTED BY DMM, DMM GETS (DPM1): DP BITS 0 ALL 1 07-35 2 00-06, 14-35 07-13 3 00-13, 21-35 14-20 4 00-13, 21-35 28-34 5 00-13, 21-35 28-34 6 ALL 7 ALL NONE NONE NONE NONE NONE NONE	34 SWEEP 38 PXCTOFF 40 INHCR/18 41 LOADIR 43 LDPI 44 ASHOV 45 EXACTY 46 EXACTY 47 BDACBLK 61 LDINST	00 CONSOLE CONSOLE DISP 12 DROM 13 AREAD 31 DPLEFT 34 NORMA 35 DP 36 ADISP 37 BDISP 41 RETURN 62 MUL 63 PAGE FAIL 64 NICOND 65 BYTE 66 EAMODE 67 SCAD 0 71 SCAD 71 SCAD 71 SCAD 71 SCAD
	PC FLAGS 00-17 NEW PI LEVEL 19-21, VMA 27-35 DATA PATH CACHE, ACS, WORKSP RAM DBM MIXER	0 S'AD DIAG 00-17, PAGE FAIL DISP 18-21, APR FLAGS 22-35 5 COPIES OF SCAD 1-7 2 EXP 3 DP 4 DPSWAP 5 VMA 6 MEM 7 #	SHSTYLE (DPE1) 0 NORM 2 40-BIT REGS 1 ZERO (LSB) 2801 2 ONES SHIF IN ONES 3 ROT ROTATE 4 ASHC ARITH SHIF* 5 LSHC LOGICAL SHIF* 6 DIV SPECIFIC DIVIDE 7 ROTC *COMBINED BYTE (DPM1) 1 BYTE 1 2 BYTE 2 3 BYTE 3 4 BYTE 4 5 BYTE 5	34 SWEEP 38 PXCTOFF 40 INHCR/18 41 LOADIR 43 LDPI 44 ASHOV 45 EXACTY 46 EXACTY 47 BDACBLK 61 LDINST	00 CONSOLE CONSOLE DISP 12 DROM 13 AREAD 31 DPLEFT 34 NORMA 35 DP 36 ADISP 37 BDISP 41 RETURN 62 MUL 63 PAGE FAIL 64 NICOND 65 BYTE 66 EAMODE 67 SCAD 0 71 SCAD 71 SCAD 71 SCAD 71 SCAD

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Microword Format (Bits 36-62)

FIELD	SKIP <63:68>			TIME CONTROL <68:71>			RANDOM CONTROL BITS <72:80>												<81:89>
	ENABLE	SELECT	NU	T00	T01	CRY 28	LOAD SC	LOAD FE	FM WRITE	MEM	DIV. IDE	MULTI PREC	MULTI SHIFT	CALL					
SIGNAL	40	20 10 4 2 1	68	70	71	72	73	74	75	76	77	78	79	80					
WORD BIT	63	64 66 67 68	12	13	25	90	91	48	28	52	53	49	14						
GRAM BIT	15	17 33 34 35																	
SLOT		12																	
PIN	BM2	CE2 CM2 BS1/2 CK1/2 CS1/2	AE2	AM2	AN/R2	DJ2	DS2	AE1	BF/J2	CE1	CN1	AM1	BE2						
DEFAULT		D = 70	F = *																
<63:89>	<p>(ICRA2,DPEA)</p> <p>04 10LGL NOT USER, USER NOT, CONSOLE EXECUTE MODE</p> <p>12 LLE AD LEFT LE 0</p> <p>21 CRY0 AD CRY.2</p> <p>32 ADLE00 ADDER LEFT = 0</p> <p>33 ADRE00 ADDER RIGHT = 0</p> <p>34 KERNEL NOT USER</p> <p>35 FPD 1ST PART DONE</p> <p>36 ACD AC NO.15 0</p> <p>37 INT INTERRUPT REQ</p> <p>42 LE AD SIGN AD EQ 0</p> <p>51 CRY2 AD CRY 02</p> <p>52 DP0 AD SIGN</p> <p>53 JFL00 USER TOP</p> <p>54 JFL01 USER BOT</p> <p>55 JFL SKIP</p> <p>56 CRY1 AD CRY 1</p> <p>57 TXXX TEST INSTRUCTION SHOULD SKIP</p> <p>61 TRAP CYCLE TRAP 1, 2, OR 3</p> <p>62 ADE00 AD EQ 0</p> <p>63 SC SC SIGN BIT</p> <p>64 EXECUTE CONSOLE EXECUTE MODE</p> <p>65 -10 BUSY NOT LATCH</p> <p>66 -10 BUSY NOT LATCH</p> <p>67 -1MS NOT CONTINUE</p> <p>68 -1MS NOT CONTINUE</p> <p>69 -1MS NOT CONTINUE</p> <p>(CSLS)</p> <p>0 2T 300 NSEC</p> <p>1 3T 450</p> <p>2 4T 600</p> <p>3 5T 750</p> <p>*- DT <108:111></p> <p>D=0</p> <p>0 2T</p> <p>1 3T</p> <p>2 4T</p> <p>3 5T</p> <p>CRY 28 INJECT A CARRY INTO 2801 ADDER</p> <p>LOAD SC LOAD STEP COUNTER FROM SCAD</p> <p>LOAD FE LOAD FE REGISTER FROM SCAD</p> <p>FM WRITE WRITE FROM FILE</p> <p>MEM WRITE FROM FILE</p> <p>DIV. IDE THIS MICROINSTRUCTION IS DOING A DIVIDE</p> <p>MULTI PREC MULTIPRECISION DIVIDE STEP</p> <p>MULTI SHIFT MULTISHIFT (NOT DPES MULTISHIFT)</p> <p>CALL CALL THIS IS A CALL</p>																		

MR 2/01

Microword Format (Bits 63-89)

= MAGIC NUMBER \ 90:107																	
-00	-01	-02	-03	-04	-05	-06	-07	-08	-09	-10	-11	-12	-13	-14	-15	-16	-17
90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107
54	55	56	57	58	59	36	37	38	39	40	41	42	43	44	45	46	47
DE1	DN1	EE1	EN1	FE1	FN1	AD1/2	AM1/2	BD1/2	BM1/2	CD1/2	CM1/2	DD1/2	DM1/2	ED1/2	EM1/2	FD1/2	FM1/2
11																	
STATE REGISTER CONTROL (NOT USED BY HARDWARE)																	
STATE \ 90:107 > (PAGE FAIL CODE)																	
0 SIMPLE																	
1 BLT																	
2 MAP IN PROGRESS																	
3 SRC																	
4 SRC-DST																	
5 SRC-DST																	
6 DSTF																	
7 CVTD8																	
8 COMP-DST																	
9 COMP-SRC																	
10 EDIT-SRC																	
11 EDIT-DST																	
12 EDIT-S+D																	
13 EDIT-D+D																	
14 BOTH SRC AND DEST POINTERS																	
AC CONTROL (DPE6)																	
AC ALU < 98:103 >																	
26 B																	
62 AC-N																	
CIN 30 34 52 51 MOD 88 84 82 81																	
(7ALS181 ON DPE6)																	
ACN \ 104:107 > AC NAMES FOR STRING INSTRUCTIONS																	
0 SRCLEN																	
1 SRCP																	
2 SRCLEN																	
3 DLEN																	
4 DSTP																	
5 MARK																	
6 BIN0																	
7 HIGH WORD OF BINARY																	
8 LOW WORD OF BINARY																	
WORKSPACE ADDRESS IN RAMFILE																	
WORK \ 98:107																	
160 BADM0																	
161 BADW1																	
200 MUL																	
201 DIV																	
210 SVMA																	
211 SVBR																	
212 SVARX																	
213 SVBRX																	
214 SVBRX																	
215 SBR																	
216 CBR																	
217 CSTM																	
220 PUR																	
221 ADJP																	
222 ADJS																	
223 ADJR																	
224 ADJ1																	
225 ADJ2																	
226 ADJRW																	
227 HSBADR																	
230 APR																	
AC BLK7 WORDS (BAD DATA FROM MEM)																	
AC BLK7 WORDS (BAD DATA FROM MEM)																	
TEMP FOR MULTIPLY																	
TEMP FOR DIVIDE																	
SAVE UBA																	
SAVE AR																	
SAVE ARX																	
SAVE BR																	
SAVE BRX																	
SPT BASE REGISTER																	
SPT BASE ADDRESS																	
CST MASK																	
PROCESS USE REGISTER																	
"P" FOR ADJBP																	
"S" FOR ADJR FOR ADJBP																	
TEMP FOR ADJBP																	
TEMP FOR ADJBP																	
BYTES/WORD FOR ADJBP																	
HALT STATUS BLOCK ADDRESS																	
APR ENABLES																	

FIELD

SIGNAL

WORD BIT

CRAM BIT

SLOT

PIN

- 90:107 -

MM 2702

Microword Format (Bits 90-107)

<p>HALT CODE</p> <p>HALT < 90:107 ></p> <p>0 - 77 NORMAL HALTS</p> <p>0 POWER UP</p> <p>1 HALT INSTRUCTION</p> <p>2 CSL CONSOLE HALT</p> <p>100 - 177 SOFTWARE ERRORS</p> <p>100 10PF 10 PAGE FAIL</p> <p>101 ILLI1 ILLEGAL INTERRUPT INSTRUCTION</p> <p>102 ILLI2 BAD PTR TO UBUS INTERRUPT VECTOR</p> <p>1000 - 1777 HARDWARE ERRORS</p> <p>1000 BHI4 ILLEGAL WRITE FUNCTION (BAD DROM)</p> <p>1004 MUCDS ILLEGAL DROM ADDRESS</p> <p>1006 MULERR VALUE COMPUTED FOR 10**21 WRONG</p> <p>1777 PAGEF PAGE FAIL IN SMALL μ CODE</p>	<p>EXTEND INSTRUCTION</p> <p>240 E0 ORIGINAL EFFECTIVE ADDRESS</p> <p>241 E1 EA OF WORD AT E0</p> <p>242 SLEN SOURCE LENGTH</p> <p>243 MSK BYTE MASK</p> <p>244 MLEN MASK LENGTH</p> <p>245 CMS SRC BYTE IN STRING COMPARE</p> <p>246 FSG SAVED ARX WHILE STORING FLOAT CHAR</p> <p>247 BDH BINARY BEING CONVERTED</p> <p>250 BDL TO DECIMAL</p> <p>TIMER STUFF</p> <p>300 TIME0 HIGH ORDER 36 BITS OF TIME</p> <p>301 TIME1 LOW ORDER 36 BITS OF TIME</p> <p>302 TIME2 TIME TO GO TO NEXT INTERRUPT</p> <p>303 TTG TIME TO GO TO NEXT INTERRUPT</p> <p>DIV STUFF</p> <p>314 AC0</p> <p>315 AC1</p> <p>316 AC2</p> <p>317 AC3</p> <p>320 DDIV SIGN</p> <p>321 DVSOR H</p> <p>322 DVSOR L</p> <p>POWERS OF TEN</p> <p>344 DECLO LOW WORD</p> <p>373 DECHI HIGH WORD</p> <p>422 YSAVE Y OF LAST INDIRECT POINTER</p> <p>423 PTAE EXEC PAGE MAP ADR (NOT PROCESS TABLE)</p> <p>424 PTAU USER PAGE MAP ADR</p> <p>425 TRAPP TRAP CYCLE SAVED PC</p> <p>426 SVARI SAVED AR</p>
<p>SCAD CONTROL (DPM3)</p> <p>SCAD - 90:82 SCADA - 93:95 SCAD8 - 96:97</p> <p>0 A*2 0 SC 0 FE</p> <p>1 A OR B 1 S 1 EXP</p> <p>2 A . B . 1 2 PTR 44 (44 & BIT 6) 2 SFT</p> <p>3 A . B 3 BYTE 2 3 S . 98:107</p> <p>4 A . B 4 BYTE 2</p> <p>5 A AND B 5 BYTE 3</p> <p>6 A . 1 6 BYTE 4</p> <p>7 A 7 BYTE 5</p>	<p>MR 2/03</p>

Microword Format (Bits 90-107)

BIT		FUNCTIONS		BIT		FUNCTIONS		
90	91	MEMORY CYCLE CONTROL (MEM BIT 76)	FORCE USER MODE REF FORCE EXEC MODE REF (PXCT) FETCH THIS IS AN INSTRUCTION FETCH	PI RIGHT BITS PIZER < 90:82 > ZERO PI1 IN PROG	PC FLAG CONTROL (DPEB) SETOV SETNOV SETNOV SETNOV CLRFPD SETFPD HOLD USER SPARE TRAP 2 TRAP 1 LD PCU SPARE SPARE	94	95	ONLY TO SETUP DP DURING DP FUNCTION PREVIOUS WHO ARE YOU CYCLE WRU CYCLE VAL 1/2R CYCLE READ INTERRUPT VECTOR BYTE CYCLE
92	93	START A READ CYCLE PAGE FAIL IF NOT WRITTEN START A MEM WRITE CYCLE (DPM 5)	PI1 IN PROG PI1P1 PI1P2 PI1P3 PI1P4 PI1P5 PI1P6 PI1P7 PI1ON PI1CO1	WRI DATA PI1MBZ < 90:83 > MUST BE ZERO PILDR PI1REQ PI1TCN PI1TCF PI1TSF PI1TSM PI1SC1	96	97	FLG BITS FLGW FLGP1 FLGC FLGSM RIGHT 1/2 OF FLG USED TO RECOVER FROM PAGE FAILS	
94	95	DO NOT LOOK IN CACHE DO NOT INVOKE PAGING HARDWARE (DPM 4)	PI1P1 PI1P2 PI1P3 PI1P4 PI1P5 PI1P6 PI1P7 PI1ON PI1CO1	PI1REQ PI1TCN PI1TCF PI1TSF PI1TSM PI1SC1	96	97	W BIT FROM PAGE MAP PI CYCLE CACHE BIT FROM PAGE MAP SPECIAL NEGATE IN FDV & DFOV FROM PAGE FAILS	
96	97	PXCT < 96:101 > WHICH PXCT BITS TO LOOK AT: 1 - E1 2 - E2 3 - D1	PI1P1 PI1P2 PI1P3 PI1P4 PI1P5 PI1P6 PI1P7 PI1ON PI1CO1	PI1TSF PI1TSM PI1SC1	98	99	APR ID DATA < 90:107 > MICROCODE OPTIONS - 90:98 - OPT 0 MICROCODE VERSION - 98:107 - UCY 101	
100	101	START A READ IF DROM ASKS IGNORE = 0:11, USE DP 0:13, DP8 - FORCE PREV LOAD THE VMA (DPE 6)	PI1CO2 PI1CO3 PI1CO4 PI1CO5 PI1CO6 PI1CO7	PI1SC2 PI1SC3 PI1SC4 PI1SC5 PI1SC6 PI1SC7	102	103		
102	103	START A READ IF DROM ASKS IGNORE = 0:11, USE DP 0:13, DP8 - FORCE PREV LOAD THE VMA (DPE 6)	PI1CO2 PI1CO3 PI1CO4 PI1CO5 PI1CO6 PI1CO7	PI1SC2 PI1SC3 PI1SC4 PI1SC5 PI1SC6 PI1SC7	104	105		
104	105	PUT VMA 14:17 ON BUS START A MEMORY CYCLE (DPM 5) START A MEMORY CYCLE IF DROM ASKS	PI1CO2 PI1CO3 PI1CO4 PI1CO5 PI1CO6 PI1CO7	PI1SC2 PI1SC3 PI1SC4 PI1SC5 PI1SC6 PI1SC7	106	107		

Microword Format (Bits 90-107)

MR 2/04

ECC (MOS MEMORY ERROR CORRECTION) BITS
 C-Field is "hidden" as (Memory status register):

MOS DATA BIT	Meaning
36	Check Bit CP
37	Check Bit C40
38	Check Bit C20
39	Check Bit C10
40	Check Bit C4
41	Check Bit C2
42	Check Bit C1

C-Field	Meaning	C-Field	Meaning
0	: Unknown ECC-CODE 0	40	: ECC Bit C40 failed
1	: ECC-Bit C1 failed	41	: Bit 18 failed
2	: ECC-Bit C2 failed	42	: Bit 19 failed
3	: Unknown ECC-CODE 3	43	: Bit 20 failed
4	: ECC-BIT C4 failed	44	: Bit 21 failed
5	: Unknown ECC-CODE 5	45	: Bit 22 failed
6	: Unknown ECC-CODE 6	46	: Bit 23 failed
7	: Unknown ECC-CODE 7	47	: Unknown ECC-CODE 47
10	: ECC-Bit C10 failed	50	: Unknown ECC-CODE 50
11	: Bit 0 failed	51	: Bit 24 failed
12	: Bit 1 failed	52	: Bit 25 failed
13	: Bit 2 failed	53	: Bit 26 failed
14	: Bit 3 failed	54	: Bit 27 failed
15	: Bit 4 failed	55	: Bit 28 failed
16	: Bit 5 failed	56	: Bit 29 failed
17	: Unknown ECC-CODE 17	57	: Unknown ECC-CODE 57
20	: ECC-Bit C20 failed	60	: Unknown ECC-CODE 60
21	: Bit 6 failed	61	: Bit 30 failed
22	: Bit 7 failed	62	: Bit 31 failed
23	: Bit 8 failed	63	: Bit 32 failed
24	: Bit 9 failed	64	: Bit 33 failed
25	: Bit 10 failed	65	: Bit 34 failed
26	: Bit 11 failed	66	: Bit 35 failed
27	: Unknown ECC-CODE 27	67	: Unknown ECC-CODE 67
30	: Unknown ECC-CODE 30	70	: Unknown ECC-CODE 70
31	: Bit 12 failed	71	: Unknown ECC-CODE 71
32	: Bit 13 failed	72	: Unknown ECC-CODE 72
33	: Bit 14 failed	73	: Unknown ECC-CODE 73
34	: Bit 15 failed	74	: Unknown ECC-CODE 74
35	: Bit 16 failed	75	: Unknown ECC-CODE 75
36	: Bit 17 failed	76	: Unknown ECC-CODE 76
37	: Unknown ECC-CODE 37	77	: Unknown ECC-CODE 77

GEN. INFO.

MEMORY ADDRESS MAP

Double spaced at 16K
Triple spaced at 64K

FROM	START	STOP	TO
0K	00	07777	4K
4K	10000	17777	8K
8K	20000	27777	12K
12K	30000	37777	16K
16K	40000	47777	20K
20K	50000	57777	24K
24K	60000	67777	28K
28K	70000	77777	32K
32K	100000	107777	36K
36K	110000	117777	40K
40K	120000	127777	44K
44K	130000	137777	48K
48K	140000	147777	52K
52K	150000	157777	56K
56K	160000	167777	60K
60K	170000	177777	64K
64K	200000	207777	68K
68K	210000	217777	72K
72K	220000	227777	76K
76K	230000	237777	80K
80K	240000	247777	84K
84K	250000	257777	88K
88K	260000	267777	92K
92K	270000	277777	96K
96K	300000	307777	100K
100K	310000	317777	104K
104K	320000	327777	108K
108K	330000	337777	112K
112K	340000	347777	116K
116K	350000	357777	120K
120K	360000	367777	124K
124K	370000	377777	128K
128K	400000	407777	132K
132K	410000	417777	136K
136K	420000	427777	140K
140K	430000	437777	144K
144K	440000	447777	148K
148K	450000	457777	152K
152K	460000	467777	156K
156K	470000	477777	160K
160K	500000	507777	164K
164K	510000	517777	168K
168K	520000	527777	172K
172K	530000	537777	176K
176K	540000	547777	180K
180K	550000	557777	184K
184K	560000	567777	188K
188K	570000	577777	192K

FROM	START	STOP	TO
192K	600000	607777	196K
196K	610000	617777	200K
200K	620000	627777	204K
204K	630000	637777	208K
208K	640000	647777	212K
212K	650000	657777	216K
216K	660000	667777	220K
220K	670000	677777	224K
224K	700000	707777	228K
228K	710000	717777	232K
232K	720000	727777	236K
236K	730000	737777	240K
240K	740000	747777	244K
244K	750000	757777	248K
248K	760000	767777	252K
252K	770000	777777	256K

GEN. INFO.

ASCII CODE

INPUT-OUTPUT CODES

Even Parity Bit	7-Bit Decimal	7-Bit Octal	Character	Remarks
0	000	000	NUL	Null, tape feed. Control shift P.
1	001	001	SOH	Start of heading [SOM, start of message]. Control A.
1	002	002	STX	Start of text [EOA, end of address]. Control B.
0	003	003	ETX	End of text [EOM, end of message]. Control C.
1	004	004	EOT	End of transmission; shuts off TWX machines and disconnects some data sets. Control D.
0	005	005	ENQ	Enquiry [WRU, "Who are you?"]. Triggers identification ("Here is...") at remote station if so equipped. Control E.
0	006	006	ACK	Acknowledge [RU, "Are you...?"]. Control F.
1	007	007	BEL	Rings the bell. Control G.
1	008	010	BS	Backspace. Control H.
0	009	011	HT	Horizontal tab. Control I.
0	010	012	LF	Line feed. Control J.
1	011	013	VT	Vertical tab. Control K.
0	012	014	FF	Form feed to top of next page. Control L.
1	013	015	CR	Carriage return to beginning of line. Control M.
1	014	016	SO	Shift out; change character set or change ribbon color to red. Control N.
0	015	017	SI	Shift in; return to standard character set or color. Control O.
1	016	020	DLE	Data link escape [DCO]. Control P.
0	017	021	DC1	Device control 1, turns transmitter (reader) on. Control Q (X ON).
0	018	022	DC2	Device control 2, turns punch or auxiliary on. Control R (TAPE, AUX ON).
1	019	023	DC3	Device control 3, turns transmitter (reader) off. Control S (X OFF).
0	020	024	DC4	Device control 4 (stop), turns punch or auxiliary off. Control T (AUX OFF).

ASCII CODE (CONT)

INPUT-OUTPUT CODES

Even Parity Bit	7-Bit Decimal	7-Bit Octal	Character	Remarks
1	021	025	NAK	Negative acknowledge [ERR, error]. Control U.
1	022	026	SYN	Synchronous idle [SYNC]. Control V.
0	023	027	ETB	End of transmission block [LEM, logical end of medium]. Control W.
0	024	030	CAN	Cancel [S ₀]. Control X.
1	025	031	EM	End of medium [S ₁]. Control Y.
1	026	032	SUB	Substitute [S ₂]. Control Z.
0	027	033	ESC	Escape, prefix [S ₃]. Control shift K.
1	028	034	FS	File separator [S ₄]. Control shift L.
0	029	035	GS	Group separator [S ₅]. Control shift M.
0	030	036	RS	Record separator [S ₆]. Control shift N.
1	031	037	US	Unit separator [S ₇]. Control shift O.

FIGURES

1	032	040	SP	Space.
0	033	041	!	
0	034	042	"	
1	035	043	#	£ on some (non-DIGITAL) units.
0	036	044	\$	
1	037	045	%	
1	038	046	&	
0	039	047	'	Accent acute or apostrophe - ' before 1965, but used until recently on DIGITAL units.
0	040	050	(
1	041	051)	
1	042	052	*	
0	043	053	+	
1	044	054	,	
0	045	055	-	
0	046	056	.	
1	047	057	/	
0	048	060	Ø	
1	049	061	1	

GEN. INFO.

ASCII CODE (CONT)

Even Parity Bit	7-Bit Decimal	7-Bit Octal	Character	Remarks
1	050	062	2	
0	051	063	3	
1	052	064	4	
0	053	065	5	
0	054	066	6	
1	055	067	7	
1	056	070	8	
0	057	071	9	
0	058	072	:	
1	059	073	;	
0	060	074	<	
1	061	075	=	
1	062	076	>	
0	063	077	?	
UPPER CASE				
1	064	100	@	1965-67, but never on DIGITAL units.
0	065	101	A	
0	066	102	B	
1	067	103	C	
0	068	104	D	
1	069	105	E	
1	070	106	F	
0	071	107	G	
0	072	110	H	
1	073	111	I	
1	074	112	J	
0	075	113	K	
1	076	114	L	
0	077	115	M	
0	078	116	N	
1	079	117	O	
0	080	120	P	
1	081	121	Q	
1	082	122	R	
0	083	123	S	
1	084	124	T	
0	085	125	U	

ASCII CODE (CONT)

Even Parity Bit	7-Bit Decimal	7-Bit Octal	Character	Remarks
0	086	126	v	
1	087	127	w	
1	088	130	x	
0	089	131	y	
0	090	132	z	
1	091	133	[Shift K.
0	092	134	\	~ 1965-67, but never on DIGITAL units. Shift L.
1	093	135]	Shift M.
1	094	136	^	Circumflex - ^ before 1965, but used until recently on DIGITAL units.
0	095	137	_	Underscore - _ before 1965, but used until recently on DIGITAL units.
LOWER CASE				Codes 140-173 first defined in 1965. For a full ASCII character set, the monitor accepts codes 140-176 as lower case. For a character set that lacks lower case, the monitor translates input codes 140-174 into the corresponding upper case codes (100-134) and translates both 175 and 176 into 033, escape. Early versions of the monitor used 175 as the escape code and translated both 176 and 033 to it.
0	096	140		Accent grave - ` @ 1965-67, but never on DIGITAL units.
1	097	141	a	
1	098	142	b	
0	099	143	c	
1	100	144	d	
0	101	145	e	
0	102	146	f	
1	103	147	g	
1	104	150	h	
0	105	151	i	
0	106	152	j	
1	107	153	k	
0	108	154	l	
1	109	155	m	
1	110	156	n	

GEN. INFO.

ASCII CODE (CONT)

Even Parity Bit	7-Bit Decimal	7-Bit Octal	Character	Remarks
0	111	157	o	
1	112	160	p	
0	113	161	q	
0	114	162	r	
1	115	163	s	
0	116	164	t	
1	117	165	u	
1	118	166	v	
0	119	167	w	
0	120	170	x	
1	121	171	y	
1	122	172	z	
0	123	173	{	
1	124	174		Control character ACK before 1965; 1965-67, but never on DIGITAL units. Vertical bar may or may not have gap, depending on font design, but generally does not on DIGITAL units.
0	125	175	}	Unassigned control character (usually ALT MODE) before 1965. Code generated by ALT MODE key on most DIGITAL units.
0	126	176	~	Control character ESC before 1965; 1965-67, but never on DIGITAL units. Code generated by ESC key on some DIGITAL units.
1	127	177	DEL	Delete, rub out (not part of lower case set).

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SW./JMP.

NOTES

CONSOLE BOARD UARTS SWITCH CONFIGURATIONS

CTY - Bottom Berg Connector - Switch pack E508 for baud rate selection.

KLINIK - Top Berg Connector - Switch pack E509 for baud rate selection.

Baud Rate	Switches					
	1	2	3	4	5*	6
110	0	0	0	0	0	0
300	0	0	1	0	1	0
600	1	0	0	0	1	0
1200	0	1	0	0	1	0
1800	0	1	0	1	1	0
2400	0	0	1	1	1	0
4800	0	1	1	0	1	0
9600	0	1	1	1	1	0

*NOTE: Switch 5 = stop bit selection
 0 = 2 stop bits
 1 = 1 stop bits.

RH11-C JUMPERS

RH11-C MASSBUS CONTROLLER

Lowest acceptable wire list Revision C

M7294-YA DATA BUFFER AND CONTROL LOCATION ABCDEF03

Lowest acceptable revision etch Rev N/A CS Rev*

Jumper	State		Comments
	Disk	Tape	
W1	OUT	OUT	Sense Unibus A Parity Error
W2	IN	IN	Sense Unibus B Parity Error
E66, Pins 1-16	IN	IN	Start Count YR Words
E66, Pins 5-12	OUT	OUT	Start Count 32 Words
E66, Pins 7-10	OUT	OUT	Start Count 16 Words
E66, Pins 2-15	IN	IN	Disable Bus B HOG Mode
E66, Pins 3-14	OUT	OUT	Enable Back-to-Back MEM Cycles
E66, Pins 4-13	OUT	IN	For Tape Subsystem Only, Otherwise Out
E66, Pins 6-11	IN	OUT	For Disk Subsystem Only, Otherwise Out

M7295 BUS CONTROL LOCATION ABCDEF02

Lowest acceptable revision etch Rev N/A CS Rev D

Jumper	State		Comments
	Disk	Tape	
W1	OUT	OUT	Address Bit 12
W2	OUT	IN	Address Bit 11
W3	OUT	OUT	Address Bit 10
W4	IN	IN	Address Bit 09
W5	OUT	OUT	Address Bit 08
W6	OUT	IN	Address Bit 07
W7	OUT	IN	Address Bit 06
W8	IN	OUT	Address Bit 05
E3, Pins 1-16	OUT	IN	16-32 Registers
E3, Pins 2-15	OUT	IN	16-32 Registers
E3, Pins 3-14	IN	OUT	1-16 Registers
E3, Pins 4-13	IN	OUT	1-16 Registers
E3, Pins 5-12	IN	OUT	16 Registers
E3, Pins 6-11	OUT	OUT	8 Registers
E3, Pins 7-10	IN	OUT	4 Registers
E3, Pins 8-9	OUT	IN	2 Registers
W11	IN	IN	Vector Bit V2
W12	IN	OUT	Vector Bit V3
W13	OUT	IN	Vector Bit V4
W14	IN	OUT	Vector Bit V5
W15	OUT	OUT	Vector Bit V6
W16	IN	IN	Vector Bit V7
W17	OUT	OUT	Vector Bit V8
W18	OUT	OUT	NPR Latency
W19	IN	IN	Maintenance (MXF Errors)

W1-18: Correspond to a base address of 776700 for disks and 772440 for tapes.

W11-W17: Correspond to a vector address of 000254 for disks and 000224 for tapes.

Jumpers on E3 are set for 20 registers for disks and 14 for tapes.

DIPS site E57 should contain priority plug BR6 (54-08780).

CAUTION

Board may not be received with proper BR plug if it is a spare.

M7296 CONTROL AND STATUS REGISTERS LOCATION EF01

Lowest acceptable revision etch Rev N/A CS Rev B.

Install jumper W1 to allow only Unibus A to be selected.

M7297 PARITY CONTROL LOCATION CD01

Lowest acceptable revision etch Rev N/A CS Rev A.

No jumpers or other configurable components.

There are two visual indicators (LEDs) for MASSBUS parity error display on this board (lit if parity error detected).

M9300 UNIBUS B TERMINATOR LOCATION AB08

Lowest acceptable revision etch Rev N/A CS Rev 0.

Jumper	State	Comments
W1	IN	Beginning of bus
W2	OUT	Not end of bus
W3	OUT	Not end of bus

There is a visual indicator (LED) for an illegal jumper configuration check (lit if illegal).

M5904 CONTROLLER TRANSCEIVER LOCATIONS CD04, CD05, CD06

Lowest acceptable revision etch Rev N/A CS Rev D.

No jumpers or other configurable component.

M688 UNIBUS POWER FAIL DRIVERS LOCATIONS E04 AND E05

Lowest acceptable revision etch Rev N/A CS Rev N/A.

No jumpers or other configurable component.

Remove M688 module from Ball-K box slot #E15 only. M688 in slot #E14 to remain.

LP20-Switches

M8586 Control Location ABCDEF02

Jumper	State	Function
W1	IN(#1),OUT(#2)	ADR BIT 4
W2	IN	ADR BIT 5
W3	IN	ADR BIT 6
W4	IN	ADR BIT 7
W5	OUT	ADR BIT 8
OFF		754 Vector = 3 OFF
W6	OUT	ADR BIT 9
W7	IN	ADR BIT 10
W8	OUT	ADR BIT 11
W9	OUT	ADR BIT 12
W10	IN(#1),OUT(#2)	VEC BIT 2
W11	IN	VEC BIT 3
W12	OUT	VEC BIT 4
W13	IN	VEC BIT 5
W14	IN	VEC BIT 6
W15	IN	VEC BIT 7
W16	IN	VEC BIT 8

W1-W9 Correspond to base ADR 775400 (UNIT #1) and 775420 (UNIT #2)
 W10-W16 Correspond to Vector 754 (#1) and 750 (#2)
 Dip site E6 contains priority plug BR4 54-0876

M8587 Data Paths

W1	OUT	Install to enable parity
W2	IN	Install for DAVFU

NOTE

Cable BC06R is connected from Berg connector J1 on the M8587 module, ribbed side toward the module (red line away from handle), to the center slot of the receptacle housing mounted in the connector tray (red line towards the connector fastener).

DUP 11 Switches

There are two switch packs on each M7867 (DUP11-DA) module. Their switch settings are as follows in order to properly configure the above address and vector assignments.

DUP11 #1			DUP11 #2		
Pack	Switch	State	Pack	Switch	State
E59	1	ON	E59	1	ON
E59	2	OFF	E59	2	ON
E59	3	ON	E59	3	OFF
E59	4	ON	E59	4	OFF
E59	5	ON	E59	5	OFF
E59	6	ON	E59	6	OFF
E59	7	N/A	E59	7	N/A
E59	8	N/A	E59	8	N/A
E113	1	ON	E113	1	OFF
E113	2	ON	E113	2	ON
E113	3	ON	E113	3	ON
E113	4	OFF	E113	4	OFF
E113	5	OFF	E113	5	OFF
E113	6	ON	E113	6	ON
E113	7	ON	E113	7	ON
E113	8	ON	E113	8	ON
E113	9	ON	E113	9	ON
E113	10	ON	E113	10	ON

There are seven jumpers on each M7867 (DUP11-DA) module. They are all factory settable for compatibility with Bell 201, Bell 208 and 209 series modems and should not have to be changed unless another type modem is used.

Should another type modem be used, the jumpers must be reconfigured so that they are compatible with the type modem used. Refer to the DUP11-DA bit synchronous interface maintenance manual (EK-DUP11-MM).

As a quick verify, the standard factory settable jumper settings are as follows.

W1	IN	W5	OUT
W2	OUT	W6	IN
W3	IN	W7	IN
W4	IN		

BR priority level 5 (priority jumper P/N 5408778).

RM03 JUMPER

This jumper should be installed during system installation.

MBA BACKPLANE
E06E1 TO E09C2

NOTE

If the jumper is not installed, the diagnostics will fail and the drive will not format a pack. This jumper grounds signal BP 144 ENB H on page D56 of the MBA print set.

D211 Switches

D211 #1		D211 #2		D211 #3		D211 #4	
Pack	Switch State	Pack	Switch State	Pack	Switch State	Pack	Switch State
E11	1 N/A	E11	1 N/A	E11	1 N/A	E11	1 N/A
E11	2 ON	E11	2 OFF	E11	2 ON	E11	2 OFF
E11	3 ON	E11	3 ON	E11	3 OFF	E11	3 OFF
E11	4 OFF	E11	4 OFF	E11	4 OFF	E11	4 OFF
E11	5 OFF	E11	5 OFF	E11	5 OFF	E11	5 OFF
E11	6 OFF	E11	6 OFF	E11	6 OFF	E11	6 OFF
E11	7 ON	E11	7 ON	E11	7 ON	E11	7 ON
E11	8 N/A	E11	8 N/A	E11	8 N/A	E11	8 N/A
E81	1 ON	E81	1 OFF	E81	1 ON	E81	1 OFF
E81	2 OFF	E81	2 ON	E81	2 ON	E81	2 OFF
E81	3 OFF	E81	3 OFF	E81	3 OFF	E81	3 ON
E81	4 OFF	E81	4 OFF	E81	4 OFF	E81	4 OFF
E81	5 OFF	E81	5 OFF	E81	5 OFF	E81	5 OFF
E81	6 OFF	E81	6 OFF	E81	6 OFF	E81	6 OFF
E81	7 OFF	E81	7 OFF	E81	7 OFF	E81	7 OFF
E81	8 OFF	E81	8 OFF	E81	8 OFF	E81	8 OFF
E81	9 OFF	E81	9 OFF	E81	9 OFF	E81	9 OFF
E81	10 OFF	E81	10 OFF	E81	10 OFF	E81	10 OFF

BR Priority Level 5 (Priority Jumper P/N 5408778)

KMC11 Switches

There are two switch packs on each M8204 module. Their switch settings are as follows.

NOTE

Each backplane slot which has an M8204 (KMC11) module installed must have the backplane wire from pin CA1 to pin CB1 of that slot removed. Should the KMC11 be removed from that slot, the wire must be re-inserted in order to guarantee that the NPG signal will be passed along the Unibus.

DD11-DK (lowest acceptable Rev B). All slots which have no quad or hex module installed must have a grant continuity card (G727) installed in row D of that slot.

Pack	KMC11 #1	Switch	State
E65		1	OFF
E65		2	OFF
E65		3	ON
E65		4	ON
E65		5	OFF
E65		6	ON
E65		7	N/A
E65		8	N/A
E116		1	ON
E116		2	ON
E116		3	OFF
E116		4	OFF
E116		5	ON
E116		6	OFF
E116		7	ON
E116		8	ON
E116		9	ON
E116		10	ON

LPR - Line Parameter Register

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WRITE (7600XX)		RCVR CLOCK		RECEIVE BAUD RATE		ODD PAR		PAR ERROR		STOP BIT		CHAR LENGT		LINE NUMBER	

NOTE: XX = 12 (DZ 0), 22 (DZ 1), 32 (DZ 2), 42 (DZ 3)

12 TURN ON RECEIVE CLOCK

<11:08>
 RECEIVE BAUD RATE
 00 = 50 05 = 300 12 = 2400
 01 = 75 06 = 600 13 = 3600
 02 = 110 07 = 1200 14 = 4800
 03 = 134 10 = 1800 15 = 7200
 04 = 150 11 = 2000 16 = 9600
 17 = 192K

07 USE ODD PARITY WHEN SET
 06 PARITY ERROR ENABLE
 05 STOP BIT 0 = 1 = 1.5 OR 2
 <04:03> CHARACTER STOP LENGTH
 00 = 5 10 = 7
 01 = 6 11 = 8
 <02:00> LINE NUMBER TO LOAD IF BIT 12 IS SET
 ALLOWS RECEIVE

MR 2643

MSR - Modem Status Register

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
READ (7600XX)		CARRIER DETECT LINES		RING INDICATOR LINES		RING INDICATOR LINES		RING INDICATOR LINES		RING INDICATOR LINES		RING INDICATOR LINES		RING INDICATOR LINES	

NOTE: XX = 16 (DZ 0), 26 (DZ 1), 36 (DZ 2), 46 (DZ 3)

MR 264B

RBUF - Receiver Buffer

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
READ (7600XX)		DATA VALID		OVER RUN		FRAME ERROR		PAR ERROR		RCVR LINE NUMBER		RECEIVE DATA BITS		RECEIVE DATA BITS	

NOTE: XX = 12 (DZ 0), 22 (DZ 1), 32 (DZ 2), 42 (DZ 3)

15 RECEIVE DATA VALID
 14 OVER RUN ERROR

10.08 RECEIVER LINE NUMBER

MR 2644

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TABLES/MAPS

NOTES

NOTES

CONSOLE

MR 2662

07	06	05	04	03	02	01	00
28	29	30	31	32	33	34	35
READ DATA							

READ (10)

MR 2663

07	06	05	04	03	02	01	00
20	21	22	23	24	25	26	27
READ DATA							

READ (11)

MR 2664

07	06	05	04	03	02	01	00
12	13	14	15	16	17	18	19
READ DATA							

READ (12)

MR 2665

07	06	05	04	03	02	01	00
04	05	06	07	08	09	10	11
READ DATA							

READ (13)

07	06	05	04	03	02	01	00
REC PE	UBA3 PE	CRAM PE	MEM PE	DP PE	CRA PE	UBA2 PE	

READ (100)

07 IF 0, CONSOLE RECEIVE PARITY ERROR
 06 IF 0, UNIBUS ADAPTER 3 PARITY ERROR
 04 IF 0, CRAM PARITY ERROR
 03 IF 0, MEMORY PARITY ERROR

02 IF 0, DATA PATH PARITY ERROR
 01 IF 0, CRA PARITY ERROR
 00 IF 0, UNIBUS ADAPTER 2 PARITY ERROR

MR 2666

07	06	05	04	03	02	01	00
01	02	03	04	05	06	07	
PRIORITY INTERRUPT REQUEST							
REFRESH ERROR							

READ (101)

07 PRIORITY INTERRUPT REQUEST 1
 06 PRIORITY INTERRUPT REQUEST 2
 05 PRIORITY INTERRUPT REQUEST 3
 04 PRIORITY INTERRUPT REQUEST 4

03 PRIORITY INTERRUPT REQUEST 5
 02 PRIORITY INTERRUPT REQUEST 6
 01 PRIORITY INTERRUPT REQUEST 7
 00 MEMORY CONTROL REFRESH ERROR B

MR 2667

07	06	05	04	03	02	01	00
AC LO	RESET	MEM BUSY	I/O BUSY	BAD DATA	COM ADR	I/O DATA	DATA

READ (102)

06 MEMORY BUSY

02 COMMAND ADDRESS

MR 2668

07	06	05	04	03	02	01	00
CTY STOP	CHAR LENGTH	REMO STOP	REMO LENGTH	DPM HALT	RUN	EXE	CONT

READ (300)

07 CTY STOP BIT
 06 CTY CHARACTER LENGTH
 05 REMOTE DIAGNOSIS STOP BIT
 04 REMOTE DIAGNOSIS CHARACTER LENGTH

MR 2670

07	06	05	04	03	02	01	00
10 INTER	NXM	BUS REQ	PE OCCUR	CSL ENAB	BOOT	DATA ACK	

READ (301)

07 10 INTERRUPT
 04 BUS REQUEST
 03 PARITY ERROR OCCURRED

MR 2671

07	06	05	04	03	02	01	00
			REMO PRO	REMO EN	REMO EN	TERM CARIR	DIAG CARIR

READ (302)

03 REMOTE PROTECT
 02 REMOTE ENABLE

01 TERMINAL CARRIER
 00 REMOTE DIAGNOSIS CARRIER

MR 2672

07	06	05	04	03	02	01	00
				CLOCK ENB	CRAM ENB	DPE/M ENB	DPM PE

READ (303)

03 RECEIVE CLOCK ENABLE
 02 CRAM CLOCK ENABLE

01 IF 0, DPE/M CLOCK ENABLE
 00 IF 0, DPM PARITY ERROR

MR 2673

07	06	05	04	03	02	01	00
UBA1 PE	UBA4 PE	PAR RIGHT	PAR LEFT	PAR ERROR	TX EMPTY	RX READY	TX READY

READ (105)

07 IF 0, UNIBUS ADAPTER 1 PARITY ERROR
 06 IF 0, UNIBUS ADAPTER 4 PARITY ERROR

MR 2669

CTY UART READ STATUS REGISTER (DATA BUFFER IS I/O 201)

07	06	05	04	03	02	01	00
DATA SET	SYNC DET	FRAME ERROR	OVER RUN	PAR ERROR	TX EMPTY	RX READY	TX READY

READ (200)

07 DATA SET READY
 06 SYNC DETECT
 05 FRAMING ERROR
 04 OVERRUN ERROR

MR 2689

REMOTE UART READ STATUS REGISTER (DATA BUFFER IS I/O 203)

07	06	05	04	03	02	01	00
DATA SET	SYNC DET	FRAME ERROR	OVER RUN	PAR ERROR	TX EMPTY	RX READY	TX READY

READ (202)

07 DATA SET READY
 06 SYNC DETECT
 05 FRAMING ERROR
 04 OVERRUN ERROR

MR 2691

WRITE (1100)

07	06	05	04	03	02	01	00
RESET	PE DET	CRM PE	DP PE	CACHE ENB	1 MSEC		

06 PARITY ERROR DETECT ENABLE
 05 CRM PARITY ERROR DETECT
 04 DATA PATH PARITY ERROR DETECT

03 CACHE ENABLE
 02 1 MSECOND ENABLE

MR 2679

WRITE (1101)

07	06	05	04	03	02	01	00
				MODEM DTR	STATE	REMO T	FAULT

03 MODEM DATA TRANSFER

01 REMOTE

MR 2680

DATA/ADDRESS

07	06	05	04	03	02	01	00
				DATA			

WRITE (1102/103)

MR 2681

DATA/ADDRESS

07	06	05	04	03	02	01	00
				DATA			

WRITE (1104/106)

MR 2682

DATA/ADDRESS

07	06	05	04	03	02	01	00
				DATA			

WRITE (106/107)

MR 2683

DATA/ADDRESS

07	06	05	04	03	02	01	00
				DATA			

WRITE (110/111)

MR 2684

DATA/ADDRESS

07	06	05	04	03	02	01	00
				DATA			

WRITE (112/113)

MR 2685

ADDRESS/DATA

07	06	05	04	03	02	01	00
				BAD DATA	COM CYC	I/O DATA	DATA CYC

WRITE (114/115)

03 BAD DATA CYCLE
 02 COMMAND ADDRESS CYCLE

01 00

I/O DATA CYCLE
 DATA CYCLE

MR 2686

07	06	05	04	03	02	01	00
CSL INT							

WRITE (1116)

00 CONSOLE INTERRUPT THE 10

MR-2687

CTY UART WRITE STATUS REGISTER (DATA BUFFER IS I/O 201)

07	06	05	04	03	02	01	00
HUNT MODE	UART RESET	REQ SEND	RESET ERROR	BREAK CHAR	RECE ENB	TERM READY	TRANS ENB

WRITE (200)

07 HUNT MODE ON (SYNC)
 06 IF 0, REQUEST TO SEND
 04 RESET ERRORS
 03 SEND BREAK CHARACTER

02 RECEIVE ENABLE
 01 IF 0, TERMINAL READY
 00 TRANSMIT ENABLE

MR-2688

REMOTE UART WRITE STATUS REGISTER (DATA BUFFER IS I/O 203)

07	06	05	04	03	02	01	00
HUNT MODE	UART RESET	REQ SEND	RESET ERROR	BREAK CHAR	RECE ENB	TERM READY	TRANS ENB

WRITE (202)

07 HUNT MODE ON (SYNC)
 06 UART RESET
 04 IF 0, REQUEST TO SEND
 03 RESET ERRORS

03 SEND BREAK - CHARACTERS
 02 RECEIVE ENABLE
 01 IF 0, TERMINAL READY
 00 TRANSMIT ENABLE

MR-2690

07	06	05	04	03	02	01	00
CRM ADDRESS LOAD	CRM WRITE	CRM LOAD	SS MODE	DP RESET	STACK RESET	CRM RESET	DATA PATH RESET

WRITE (204)

04 CRM ADDRESS LOAD
 03 SINGLE STEP MODE

MR-2674

07	06	05	04	03	02	01	00
TRAP ENB				DIAGNOSTIC FUNCTIONS			

WRITE (205)

04 TRAP ENABLE

MR-2675

07	06	05	04	03	02	01	00
SINGL CLOCK						SINGL CLOCK RUN	

WRITE (206)

01 SINGLE CLOCK

MR-2676

07	06	05	04	03	02	01	00
CHECK NXM	CSL REQ	TENB C/A	TENB DC	CRA TCLK	CRA RCLK	DATA SENT	CLK ENB

WRITE (210)

06 CONSOLE REQUEST
 05 T ENABLE FOR COMMAND ADDRESS CYCLE
 04 T ENABLE FOR DATA CYCLE
 03 C/R T CLOCK

02 C/R R CLOCK
 01 LATCH DATA SENT
 00 IF 0, R CLOCK ENABLE

MR-2678

07	06	05	04	03	02	01	00
EXECUTE				RUN		CONT	

WRITE (212)

01 EXECUTE

00 CONTINUE

MR-2677

PROC. TABLES

EXECUTIVE PROCESS TABLE	
0	NOT USED
41	
42	STANDARD PRIORITY INTERRUPT INST
57	
60	NOT USED
77	
100	VECTOR INTERRUPT TABLE POINTERS
117	
120	NOT USED
177	
200	EXEC PAGE 400
377	EXEC PAGE 776
400	EXEC PAGE 401
	EXEC PAGE 777
420	NOT USED
421	EXEC ARITHMETIC OVF TRAP INST
422	EXEC STACK OVF TRAP INST
423	EXEC TRAP 3 TRAP INST
424	
	NOT USED
577	
600	EXEC PAGE 0
757	EXEC PAGE 336
760	EXEC PAGE 1
777	EXEC PAGE 337
	NOT USED

MR 2652

TOPS-10 PROCESS TABLE CONFIGURATION

USER PROCESS TABLE	
0	USER PAGE 0 USER PAGE 1
377	USER PAGE 776 USER PAGE 777
400	EXEC PAGE 340 EXEC PAGE 341
417	EXEC PAGE 376 EXEC PAGE 377
420	ADDRESS OF LUUO BLOCK
421	USER ARITHMETIC OVF TRAP INST
422	USER STACK OVF TRAP INST
423	USER TRAP 3 TRAP INST
424	MUO STORED HERE
425	PC WORD OF MUO STORED HERE
426	PROCESS CONTEXT WORD STORED HERE
427	NOT USED
430	EXEC NO TRAP MUO NEW PC WORD
431	EXEC TRAP MUO NEW PC WORD
432	NOT USED
433	
434	USER NO TRAP MUO NEW PC WORD
435	USER TRAP MUO NEW PC WORD
436	NOT USED
477	
500	EXEC OR USER PAGE FAIL WORD STORED HERE
501	EXEC OR USER OLD PC WORD STORED HERE
502	PAGE FAIL NEW PC WORD
503	
	NOT USED
777	

TOPS -10 PROCESS TABLE CONFIGURATION (CONT)

PROC. TABLES

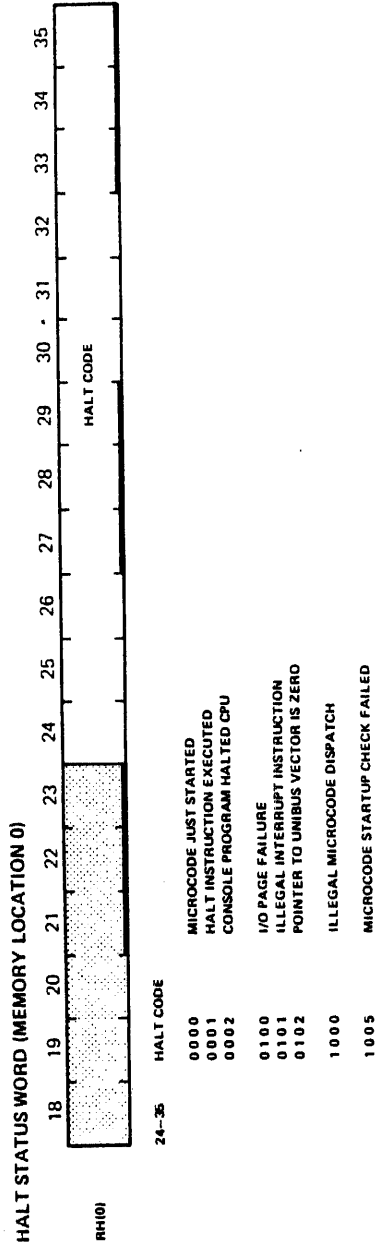
EXECUTIVE PROCESS TABLE	
0	NOT USED
41	
42	STANDARD PRIORITY INTERRUPT INST
57	
60	NOT USED
77	
100	VECTOR INTERRUPT TABLE POINTERS
117	
120	NOT USED
420	
421	EXEC ARITHMETIC OVF TRAP INST
422	EXEC STACK OVF TRAP INST
423	EXEC TRAP 3 TRAP INST
424	
	NOT USED
537	
540	EXEC SEC 0 PTR
541	
	NOT USED
777	

MR 2653

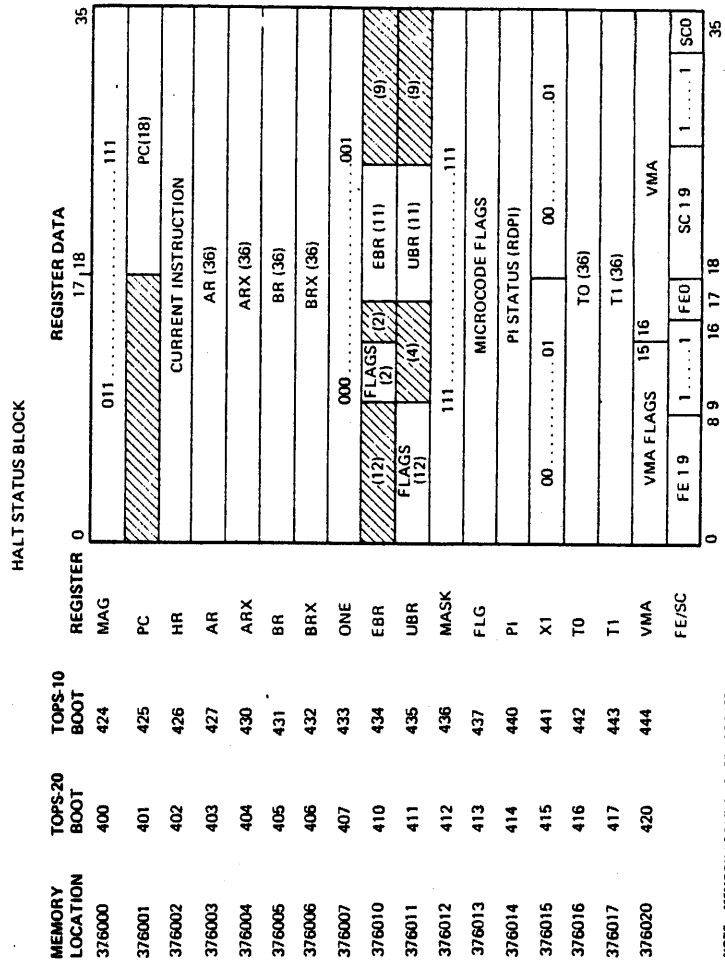
TOPS-20 PROCESS TABLE CONFIGURATION

USER PROCESS TABLE			
0	NOT USED		
420			
421		USER ARITHMETIC OVF TRAP INST	
422		USER STACK OVF TRAP INST	
423		USER TRAP 3 TRAP INST	
424		FLAGS 1 MUUO OP AC	
425		MUUO OLD PC	
426		E OF MUUO	
427		MUUO PROCESS CONTEXT WORD	
430		EXEC NO TRAP MUUO NEW PC WORD	
431		EXEC TRAP MUUO NEW PC WORD	
432		NOT USED	
433			
434		USER NO TRAP MUUO NEW PC WORD	
435		USER TRAP MUUO NEW PC WORD	
436		NOT USED	
477			
500		PAGE FAIL WORD	
501		PAGE FAIL FLAGS	
502		PAGE FAIL OLD PC	
503		PAGE FAIL NEW PC	
504		NOT USED	
537			
540			USER SEC 0 PTR
541			
777		NOT USED	

TOPS-20 PROCESS TABLE CONFIGURATION (CONT)

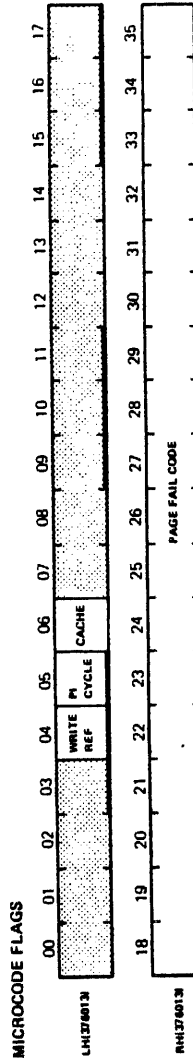


MIN 2879



NOTE: MEMORY LOCATION BASE ADDRESS MAY BE CHANGED WITH WMSB INSTRUCTION.

MR 2654



NOTE: ADDRESS MAY BE CHANGED WITH WRMB INSTRUCTION.

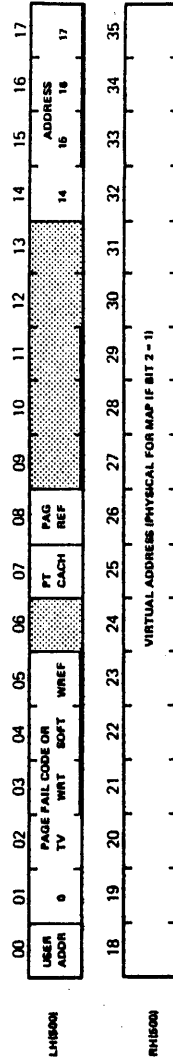
- 4 WRITE REFERENCE BIT FROM PAGE MAP
- 5 PM CYCLE
- 6 LOOK IN CACHE BIT FROM PAGE MAP

18-38 PAGE FAIL CODE

- 000000 SIMPLE INSTRUCTIONS
- 000001 BLT IN PROGRESS
- 400002 MAP IN PROGRESS
- 000003 MOVE STRING SOURCE IN PROGRESS
- 000004 MOVE STRING FILL IN PROGRESS
- 000005 MOVE STRING DESTINATION IN PROGRESS
- 000006 FILLING DESTINATION
- 000007 EDIT SOURCE
- 000010 EDIT DESTINATION
- 000011 CONVERTING DECIMAL TO BINARY
- 000012 COMPARING DECIMAL TO BINARY

MR 2025

PAGE FAIL WORD (OR MAP AC)

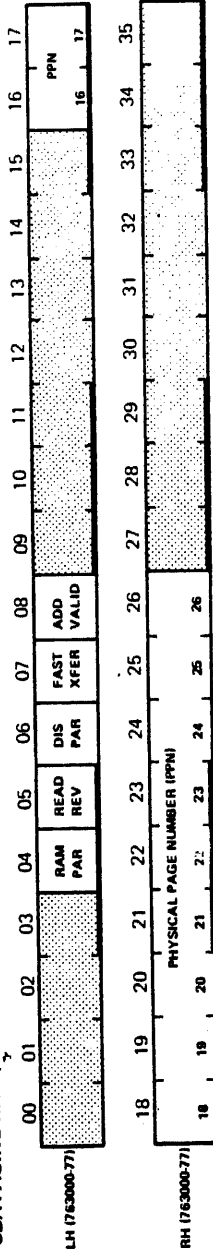


NOTE: ADDRESS IS LOCATION 000 IN I/PT.

- 0 USER ADDRESS
 - 2-5 (BIT 1 = 0) TRANSLATION VALID
 - 3 WRITABLE (I/L PAGING MODE = 0)
 - 4 WRITTEN (I/L PAGING MODE = 1)
 - 4 SOFTWARE (I/L PAGING MODE = 0)
 - 5 WRITABLE (I/L PAGING MODE = 1)
 - 5 WRITE REFERENCE
-
- 2-5 (BIT 1 = 1) PAGE FAIL CODE
 - 20 AN I/O INSTRUCTION SELECTED A NONEXISTENT DEVICE OR REGISTER. (BITS 14-20 = I/O ADDRESS)
 - 26 HARD MEMORY ERROR
 - 27 NMM
 - 7 PAGE TABLE CACHE
 - 8 PAGE REFERENCE
 - 18-25 VIRTUAL ADDRESS PHYSICAL FOR MAP IF (BIT 2 = 1)

MR 2828

UBA PAGING RAM (READ)

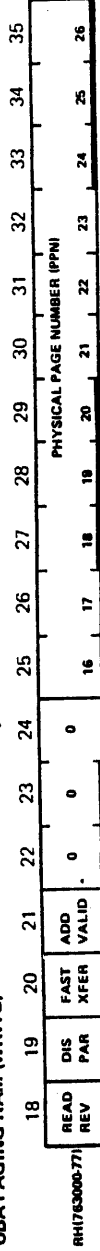


NOTE: ALL BITS READ ONLY.

- BIT(S) FUNCTION
- 04 PAGING RAM PARITY BIT
- 06 READ REVERSE
- 06 DISABLE PARITY BIT XFER TO UNIBUS
- 07 FAST TRANSFER MODE
- 08 ADDRESS IS VALID
- 08 MBZ (MUST BE ZERO)
- 16-26 PHYSICAL PAGE NUMBER

MR 2657

UBA PAGING RAM (WRITE)

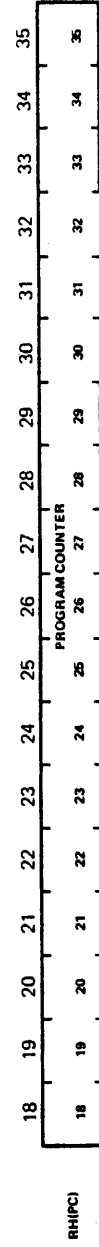
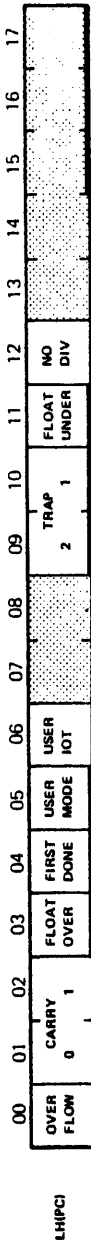


NOTE: ALL BITS WRITE ONLY.

- 18 READ REVERSE
- 19 DISABLE PARITY BIT TRANSFER TO UNIBUS
- 20 FAST TRANSFER MODE
- 21 ADDRESS IS VALID
- 21-26 MUST BE ZERO

MR 2656

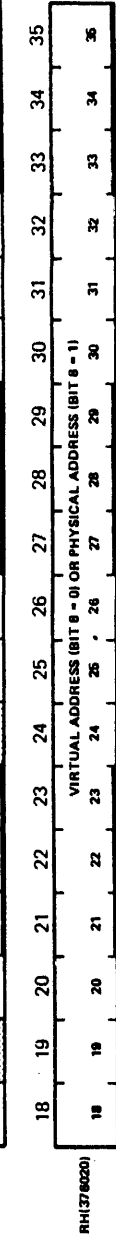
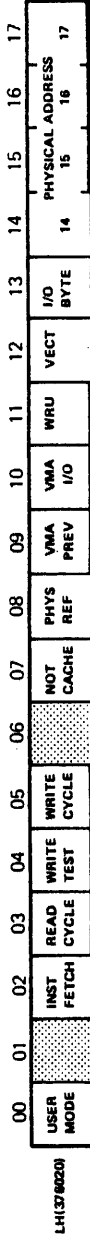
PC WORD



- 0 OVERFLOW
- 1 CARRY 0
- 2 CARRY 1
- 3 FLOATING OVERFLOW
- 4 FIRST PART DONE
- 5 USER MODE
- 6 USER IOT (ALSO PCU)
- 9 TRAP 2
- 10 TRAP 1
- 11 FLOATING UNDERFLOW
- 12 NO DIVIDE
- 18-35 PROGRAM COUNTER

MR 2827

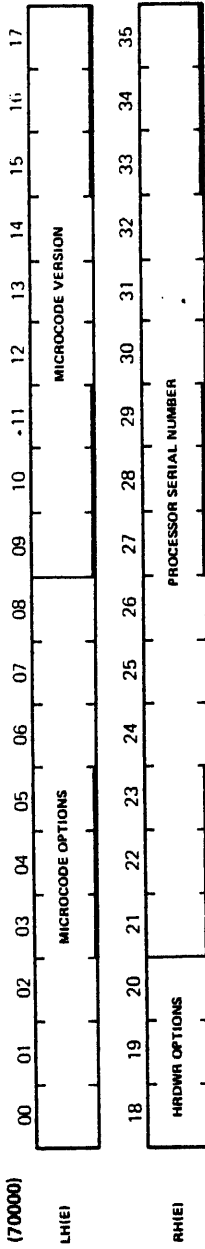
VMA



- 0 USER MODE
- 2 INSTRUCTION FETCH
- 3 READ CYCLE
- 4 WRITE TEST
- 5 WRITE CYCLE
- 7 DO NOT LOOK IN CACHE
- 8 PHYSICAL REFERENCE
- 9 VMA PREVIOUS
- 10 VMA I/O
- 11 WHO ARE YOU
- 12 VECTOR
- 13 I/O BYTE INSTRUCTION
- 14-17 BITS 14-17 OF PHYSICAL ADDRESS (OR 0)
- 18-35 BITS 18-35 OF VIRTUAL ADDRESS (BIT 8 - 0) OR PHYSICAL ADDRESS (BIT 8 - 1)

MR 2826

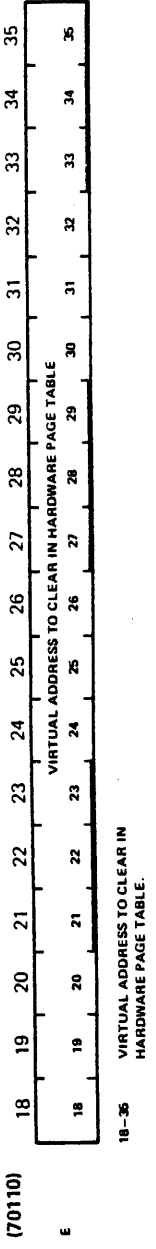
APRID -- Read Processor ID
(70000)



0-8 RESERVED FOR MICROCODE VERSION
9-17 MICROCODE VERSION NUMBER
18-20 HARDWARE OPTIONS (BITS CURRENTLY = 0)
21-35 PROCESSOR SERIAL NUMBER.

MR 2801

CLRPT -- Clear Page Table
(70110)



MR 2807

RDAPR - Read Processor Conditions
(70024)

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17		
LWIEI								PWRF		NXM		HERR		SERR		TIMER		8080	

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35				
POWER FAIL								NXM		HARD ERROR		SOFT ERROR		TIMER DONE		8080		INT REQ		PI LEVEL	

NOTE: PAGE FAIL OCCURS IF ERROR IS RESULT OF CPU MEMORY REQUEST. NXM FLAG ALSO SETS IN UNIBUS DEVICE IF ERROR IS RESULT OF UNIBUS NPM REQUEST.

- 08 POWER FAIL ENABLED
- 09 NONEXISTENT MEMORY ERROR ENABLED
- 10 HARD MEMORY ERROR INTERRUPT ENABLED
- 11 SOFT MEMORY ERROR INTERRUPT ENABLED
- 12 INTERVAL TIMER ENABLED
- 13 8080 CONSOLE INTERRUPT ENABLED
- 26 POWER FAIL ERROR
- 27 NONEXISTENT MEMORY ERROR
- 28 HARD MEMORY ERROR (CANNOT BE CORRECTED BY ECC)
- 29 SOFT MEMORY ERR (CORRECT DATA PLACED ON BUS)
- 30 INTERVAL TIMER DONE
- 31 8080 CONSOLE INTERRUPT
- 32 INTERRUPT REQUESTED
- 33-35 PIA

MR 2803

WRAPR - Write Processor Conditions
(70020)

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35								
ENAB		DISAB		CLEAR		SET		INT 8080		PWRF		NXM		SELECT FLAG HERR		SERR		TIMER		8080		INT REQ		PI LEVEL	

- 20 ENABLE CONDITIONS SELECTED BY BITS 26-31 TO CAUSE INTERRUPTS.
- 21 DISABLE INTERRUPTS FOR CONDITIONS SELECTED BY BITS 26-31.
- 22 CLEAR FLAGS INDICATED BY BITS 26-31.
- 23 SET FLAGS INDICATED BY BITS 26-31.
- 25 INTERRUPT 8080 CONSOLE
- 26 POWER FAIL
- 27 NONEXISTENT MEMORY ERROR
- 28 HARD MEMORY ERROR (CANNOT BE CORRECTED BY ECC)
- 29 SOFT MEMORY ERROR (CORRECT DATA PLACED ON BUS)
- 30 INTERVAL TIMER
- 31 8080 CONSOLE
- 32 GENERATE INTERRUPT REQUEST
- 33-35 PIA

MR 2802

**RDCSB – Read Core Status Table Base Register
(70204)**

LHIE	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
														14	15	16	17	
	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
RHIE	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35

14-35 CST (CORE STATUS TABLE) BASE REGISTER

MR 2811

**WRCSB – Write Core Status Table Base Register
(70244)**

LHIE	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
														14	15	16	17	
	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
RHIE	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35

18-35 CST (CORE STATUS TABLE) BASE REGISTER

MR 2821

RDCSTM -- Read Core Status Table Mask Register
(70214)

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17

LHIE)

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35

RHIE)

0-35 CST (CORE STATUS TABLE) MASK REGISTER

MR 2816

WRCSTM -- Write Core Status Table Mask Register
(70254)

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17

LHIE)

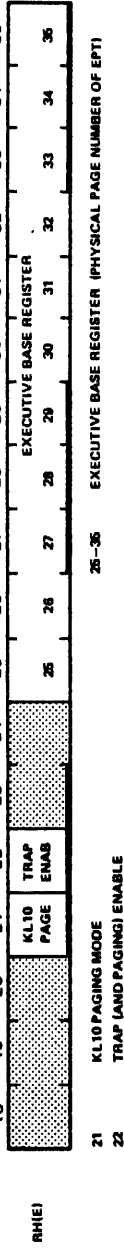
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35

RHIE)

0-35 CST (CORE STATUS TABLE) MASK REGISTER

MR 2823

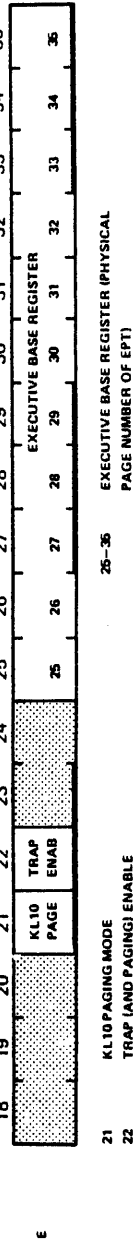
**RDEBR -- Read Executive Base Register
(70124)**



21 KL10 PAGING MODE
22 TRAP (AND PAGING) ENABLE

MR-2810

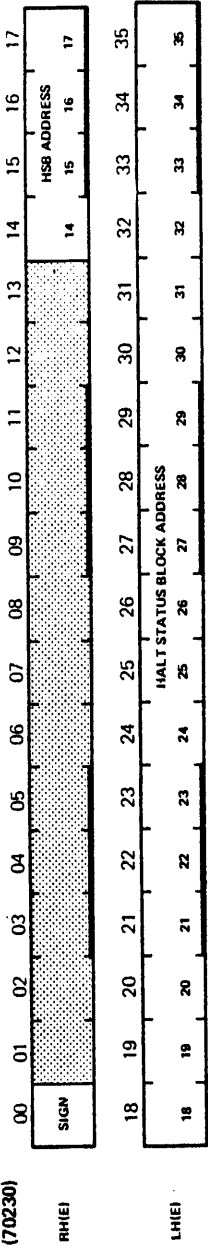
**WREBR -- Write Executive Base Register
(70120)**



21 KL10 PAGING MODE
22 TRAP (AND PAGING) ENABLE

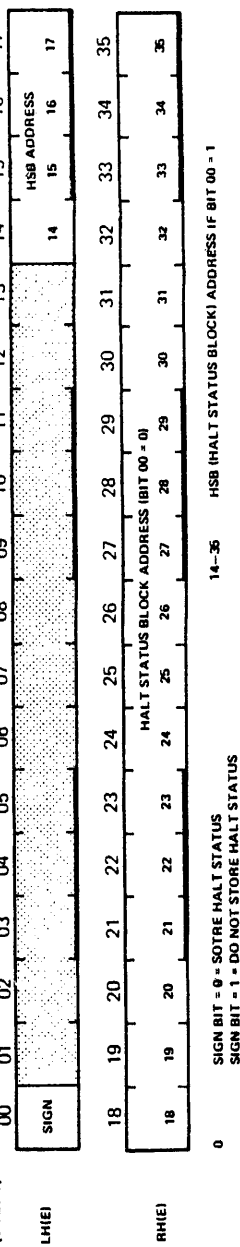
MR-2809

RDHSB - Read Halt Status Block Address (70230)



MR 2819

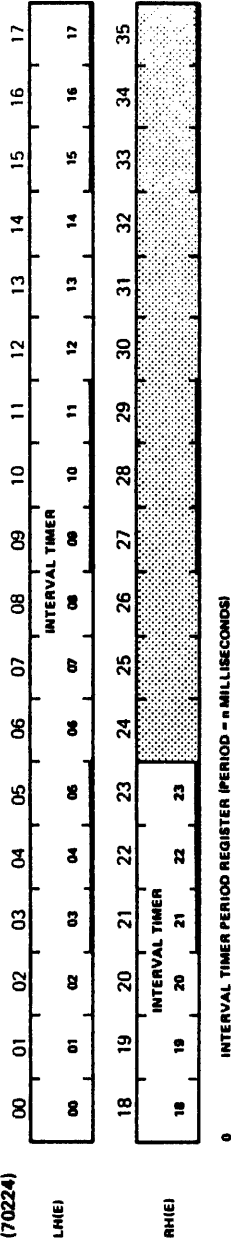
WRHSB - Write Halt Status Block Address (70270)



MR 2824

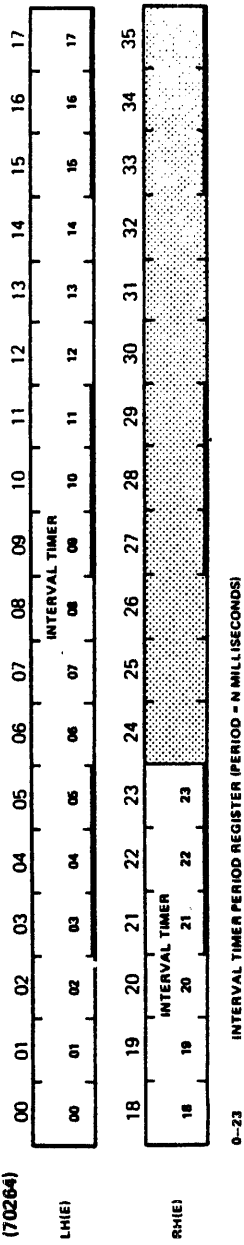
INT. TIMER

**RDINT - Read Interval Timer
(70224)**



MR 2819

**WRINT - Write Interval Timer
(70264)**



MR 2815

**RDPI - Read PI System Status
(70064)**

LHIEI	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
											PROGRAM REQUESTS							
											01	02	03	04	05	06	07	

RHIE'

	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35						
											PI IN PROGRESS		SYS ON		CHANNELS ON									
											01	02	03	04	05	06	07	01	02	03	04	05	06	07

11-17 PROGRAM REQUESTS ON CHANNELS 1-7
21-27 INTERRUPTS HOLDING (IN PROGRESS) ON CHANNELS 1-7
28 PI SYSTEM ON
29-35 ACTIVE CHANNELS 1-7.

MR 2805

**WRPI - Write PI System Conditions
(70060)**

E	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	
											DROP PROGRAM REQUESTS ON SELECTED CHANNELS.		PI SYS ON		SELECT CHANNEL				
											01	02	03	04	05	06	07		

22 DROP PROGRAM REQUESTS ON SELECTED CHANNELS.
23 CLEAR PI SYSTEM
24 INITIATE INTERRUPTS ON THE SELECTED CHANNELS.
25 TURN ON THE SELECTED CHANNEL.
26 TURN OFF THE SELECTED CHANNEL.
27 DEACTIVATE THE PI SYSTEM.
28 ACTIVATE THE PI SYSTEM.
29-35 SELECT CHANNELS FOR BITS 22, 24, 26, AND 28.

MR 2804

RDPUR – Read Process Use Register (70210)

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	
PROCESS USE REGISTER																		
LH(E)	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
RH(E)	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35

0-35 PUR (PROCESS USE REGISTER)

MR 2013

WRPUR – Write Process Use Register (70250)

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	
PROCESS USE REGISTER																		
LH(E)	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
RH(E)	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35

0-35 PUR (PROCESS USE REGISTER)

MR 2022

**RDSPB – Read Shared Pointer Table Base Register
(70200)**

LHIE)	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
															14	15	16	17
															SPT			

RHIE)

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
SHARED POINTER TABLE BASE REGISTER																	
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35

14-35 SPT (SHARED POINTER TABLE) BASE REGISTER

MIR 2812

**WRSPB – Write Shared Pointer Table Base Register
(70240)**

LHIE)	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
															14	15	16	17
															SPT			

RHIE)

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
SHARED POINTER TABLE BASE REGISTER																	
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35

14-35 SPT (SHARED POINTER TABLE) BASE REGISTER

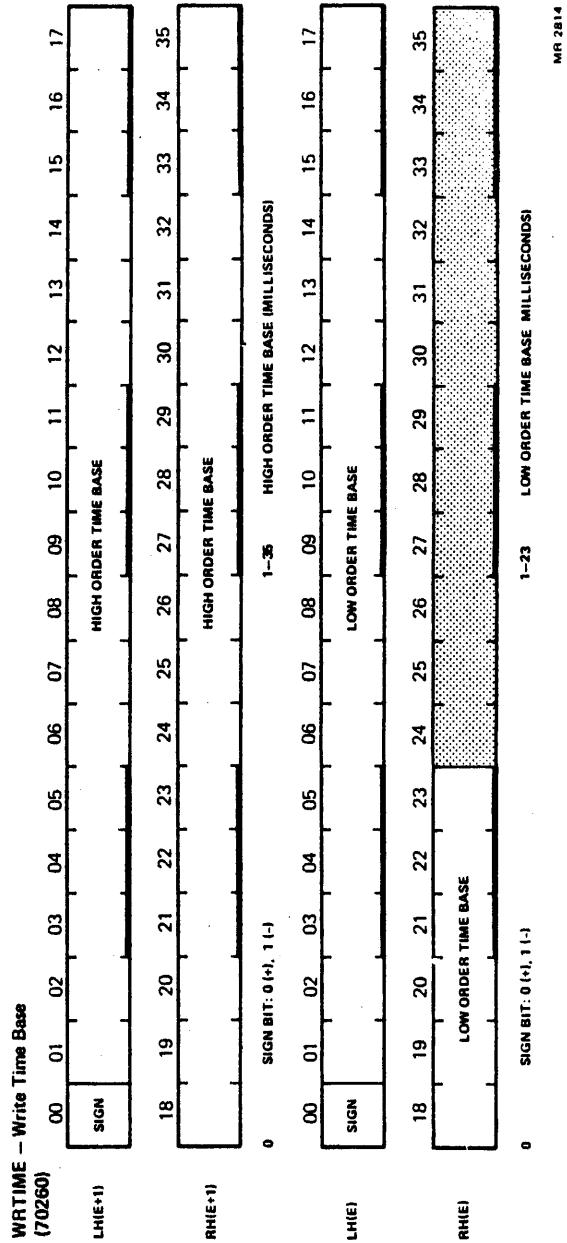
MIR 2820

TIME BASE

**RDTIME - Read Time Base
(70220)**

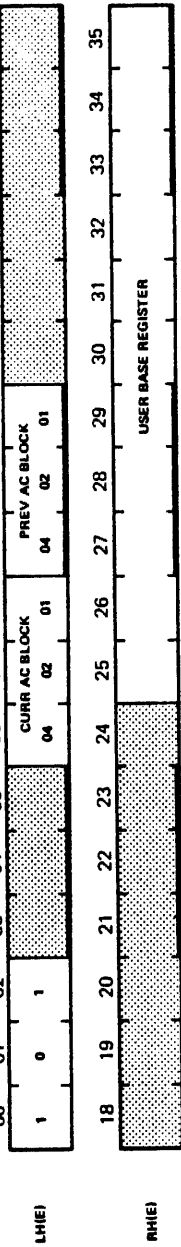
00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17		
SIGN		01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	
HIGH ORDER TIME BASE																			
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35		
SIGN		18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
HIGH ORDER TIME BASE																			
0	SIGN BIT: 0 (+), 1 (-)																		
00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17		
SIGN		01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	
LOW ORDER TIME BASE																			
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35		
SIGN		18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
LOW ORDER TIME BASE																			
0	SIGN BIT: 0 (+), 1 (-)																		
1-23	LOW ORDER TIME BASE (MILLISECONDS)																		
24-36	TIME BASE FRACTION																		

MR 2817



MR 2814

**RDUBR -- Read User Base Register
(70104)**

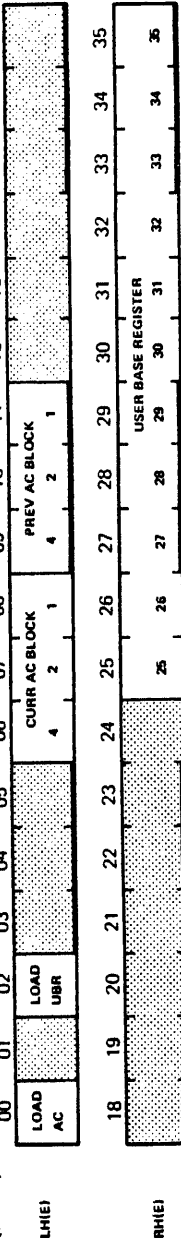


0 1
1 0
2 1

6-8 CURRENT AC BLOCK
9-11 PREVIOUS AC BLOCK
25-35 USER BASE REGISTER (PHYSICAL PAGE NUMBER OF UPT)

MR 2806

**WRUBR -- Write User Base Register
(70114)**



0 1
2 1

0 LOAD AC BLOCK NUMBERS
2 LOAD UBR
6-8 CURRENT AC BLOCK

9-11 PREVIOUS AC BLOCK
25-35 USER BASE REGISTER (PHYSICAL PAGE NUMBER OF UPT)

MR 2808

MEMORY STATUS REGISTER

LH (1000000)	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
	HOLD	BAD DATA	REF ERR	PAR ERR	ECC ON	CP	C-40	C20	C10	C04	C02	C01	PWR FAIL				ERA	
	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
PH (1000000)	ERA (ERROR ADDRESS)																	

NOTE: WRITING A 1 BIT IN 00, 02, 12 CLEARS THE FLAG.
 WRITING A 1 BIT IN 03 SETS THE FLAG, WRITING A 0 BIT CLEARS THE FLAG.

- 00 ERROR HOLD (ERROR CONDITION DETECTED BY CONTROLLER)
- 01 BAD DATA (UNCORRECTABLE READ ERROR)
- 02 REFRESH ERROR (INCOMPLETE WRITE CYCLE)
- 03 BUS PARITY ERROR DETECTED
- 04 ERROR CORRECTION ENABLED
- 05-11 CORRECTION CODE BITS
- 12 POWER FAIL (LOSS OF POWER OR BATTERY BACKUP LOW)
- 14-36 ERROR ADDRESS

MR-2660

UBA STATUS REGISTER

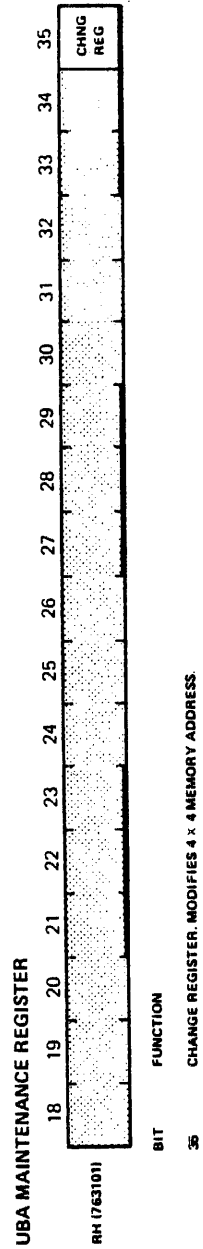
RH (763100)	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
	TIME OUT	BAD MDATA	BUS PE	NXD	HI INT	LO INT	ACDC LO	DIS XFR	INIT UBA	HIGH LEVEL PIA	LOW LEVEL PIA							
	R/W	R/W	R/W	R/W	R	R	R	R/W	W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

NOTE: WRITING A 1 BIT IN 18, 19, 20, 21 CLEARS THE FLAG.

- 18 UNIBUS ARBITRATOR TIME-OUT OR NONEXISTENT MEMORY ADDRESS.
- 19 KS10 (BACKPLANE) BUS PARITY ERROR
- 20 NONEXISTENT DEVICE
- 21 HIGH LEVEL INTERRUPT PENDING (BR7 AND BR6)
- 24 LOW LEVEL INTERRUPT PENDING (BR5 AND BR4)
- 26 AC OR DC LOW
- 28 DISABLE TRANSFER IF BMD (BIT 19 - 1).
- 29 INITIALIZE UBA AND UNIBUS DEVICES
- 30-32 HIGH LEVEL PIA
- 33-36 LOW LEVEL PIA

MR-2659

UBA MAINT



RH11 - RMWC - Word Count Register

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
WORD COUNT REGISTER																
(779702)	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

MR-2582

NOTE: ALL BITS READ/WRITE

RH11 - RMCS1 - Control and Status Register 1

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(779700)	(MIB-00)	SPEC COND	XFER ERROR	MBUS C PE	DRIVE AVAIL	PORT SEL	ADDRESS 17 16	READY	INIT ENAB	FUNCTION	GO				
R	R/W	R	R	R	R	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

NOTE: SHARED REGISTER BITS - 15, 13, AND 10-06 - ARE IN RH.
REFER TO DCL PRINT RG3 AND RG6.

- 15 SPECIAL CONDITION
- 14 TRANSFER ERROR
- 13 MASSBUS CONTROL PARITY ERROR
- 11 DRIVE AVAILABLE

- 10 PORT SELECT
- 09 UNIBUS ADDRESS EXTENSION BITS 17 AND 16
- 06 INTERRUPT ENABLE

MR-2583

RH11 - RMDS - Drive Status

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(77972)	(MIB-01)	ATTN ACT	ERROR	PIP	MOL	WRITE LOCK	LAST BLOCK	PROG ABLE	DRIVE PRES	DRIVE READY	VALID VOL				

NOTE: ALL BITS READ ONLY.
REFER TO DCL PRINT RG6.

- 15 ATTENTION ACTIVE
- 13 POSITIONING IN PROGRESS
- 12 MEDIUM ON LINE
- 10 LAST BLOCK TRANSFERRED

- 08 PROGRAMMABLE
- 08 DRIVE PRESENT
- 06 VALID VOLUME

RH11 - RMER1 - Error Register 1

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DATA CHECK	UN SAFE	OPER INC	DR T ERROR	WR LK ERROR	I ADR ERROR	A OV ERROR	H CRC ERROR	H COM ERROR	ECC ERROR	WR CK FAIL	FMT ERROR	PAR ERROR	RMR	ILL REG	ILL FUNC

(776714)
(MB-02)

NOTE: ALL BITS READ/WRITE.
REFER TO DCL PRINT RGO.

- 13 OPERATION INCOMPLETE
- 12 DRIVE TIMING ERROR
- 11 WRITE LOCK ERROR
- 10 INVALID ADDRESS ERROR
- 09 ADDRESS OVERFLOW ERROR
- 08 HEADER CRC ERROR
- 07 HEADER COMPARE ERROR
- 06 ECC HARD ERROR
- 05 WRITE CLOCK FAIL
- 04 FORMAT ERROR
- 03 PARITY ERROR
- 02 REGISTER MODIFICATION REFUSED
- 01 ILLEGAL REGISTER
- 00 ILLEGAL FUNCTION

MR 2584

RH11 - RMMR1 - Maintenance Register ONE

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OCCUP GO	RUN GO	END BLOCK	RX EXCPT	ENB SEARCH	LOOK SYNC	CRC OUT	PACK DATA	PACK HEADR	CONT	PROM STROB	ENB ECC	WRITE DATA	LAST SECTR	LAST SBT	DIAG MODE

(776724)
(MB-03)

- 15 OCCUPIED
- 14 RUN AND GO
- 13 END OF BLOCK LEVEL
- 12 RECEIVED EXCEPTION
- 11 ENABLE SEARCH
- 10 PACK LOOKING FOR SYNC
- 09 ENABLE CRC OUT
- 08 PACK DATA AREA
- 07 PACK HEADER AREA
- 06 CONTINUE
- 05 PROM STROBE
- 04 ENABLE ECC OUT
- 03 WRITE DATA
- 02 LAST SECTOR
- 01 LAST SECTOR AND TRACK
- 00 DIAGNOSTIC MODE

MR 2588

RH11 - RIMAS - Attention Summary

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
								07	06	05	04	03	02	01	00
								DRIVE ATTENTION SUMMARY							
(77/6716)	(MB-04)														

NOTE: ALL BITS READ/WRITE.
REFER TO DCL PRINT DF.

MR 2585

RH11 - RMDA - Desired Track/Sector Address

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
				TRACK ADDRESS											
				04	02	01									
				SECTOR ADDRESS											
						16	08	04	02						
(77/6706)	(MB-06)														

NOTE: ALL BITS READ/WRITE.

MR 2590

RH11 - RMDT - Drive Type

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
		MOVE HEAD				DRIVE REQ									
		DRIVE TYPE													
				06	07	06	06	04	03	02	01				
(77/6726)	(MB-08)														

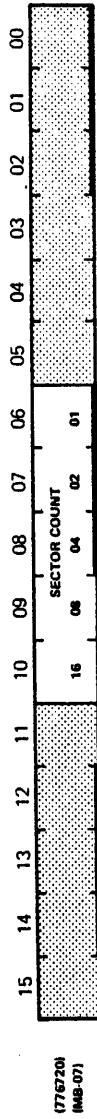
NOTE: ALL BITS READ ONLY.
REFER TO DCL PRINT ECB.

15 NOT BLOCK ADDRESSED
14 TAPE DRIVE

13 MOVING
11 DRIVE REQUEST REQUIRED

MR 2591

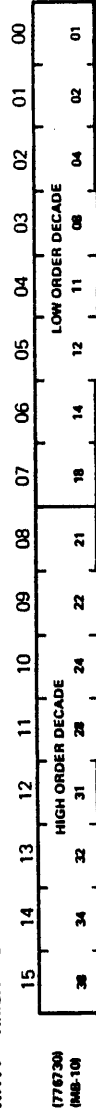
RH11 - RMLA - Look Ahead



NOTE: ALL BITS READ ONLY.

MR 2592

RH11 - RMSN - Serial Number



NOTE: ALL BITS READ ONLY.

MR 2593

RH11 - RMOF - Offset



NOTE: ALL BITS READ/WRITE.
REFER TO DCL PRINT RG1.

12 FORMAT 16 SECTORS
11 ECC INHIBIT

10 HEADER COMPARE INHIBIT
07 OFFSET DIRECTION

MR 2594

RH11 - RMDC - Desired Cylinder

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(776734) (MB-12)						DC 512	DC 256	DC 128	DC 64	DC 32	DC 16	DC 8	DC 4	DC 2	DC 1

NOTE: ALL BITS READ WRITE.
REFER TO DCL PRINT SS1.

MR 2595

RH11 - RMHR - Current Cylinder Address

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(776734) (MB-13)															

NOTE: UNUSED

MR 2596

RH11 - RMMR2 - Maintenance Register Two

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(776740) (MB-14)	REG A	REG B	CONTR TAG	CONTR BRNCH	CONTR TAG	HEAD TAG					BUS IN LINES				

NOTE:
15 REQUEST ON PORT A
14 REQUEST ON PORT B
13 CONTROL SELECT TAG
12 COMMAND SEQUENCER IS BRANCHING
11 CONTROL SELECT OR CYLINDER SELECT TAG
10 CONTROL SELECT OR HEAD SELECT TAG

0	1	2	3	4	5	6	7	8	9	CYLINDER ADDRESS TAG	HEAD SELECT TAG	CONTROL SELECT TAG
	1	2	4	8	16	32	64	128	512	1	1	1
	WRITE GATE	READ GATE	SERVO OFFSET PLUS	SERVO OFFSET PLUS	FAULT CLEAR	NOT USED	RETURN TO ZERO	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED

MR-2587

RH11 - RMMR2 - Error Register 2



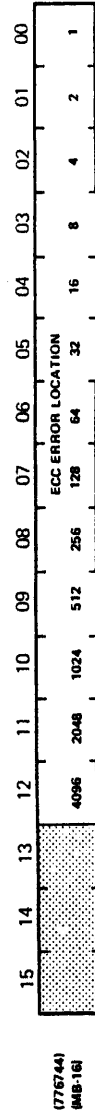
NOTE: ALL BITS READ/WRITE

- 12 INVALID COMMAND
- 11 LOSS OF SYSTEM CLOCK
- 10 LOSS OF BIT CHECK

- 07 DC OF HEAD SELECT FAULT
- 03 DATA PARITY ERROR RECEIVED

MR 2598

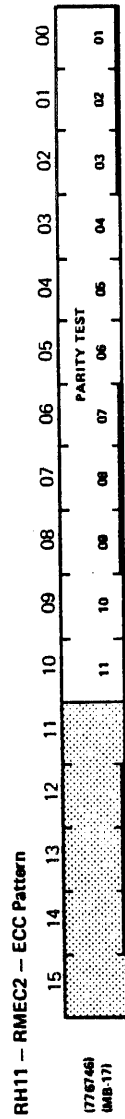
RH11 - RMEC1 - ECC Position Register 1



NOTE: ALL BITS READ ONLY.

<12:00> BURST LOCATION CODE FOR ECC

MR 2586



NOTE: ALL BITS READ ONLY.
REFER TO DCL PRINT EC1.

<10:00> PARITY TEST

MR 2587

RH11 – RPCS1 – Control and Status Register 1

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
076700 (MB-00)	SPEC COND	XFER ERROR	MBUS CPE	DRIVE AVAIL	PORT SEL	ADDRESS 17 16	READY	INIT ENAB	FUNCTION	GO	R/W	R/W	R/W	R/W	R/W

NOTE: SHARED REGISTER BITS <15:13> AND <10:06> ARE IN RH.

- 15 SPECIAL CONDITION
- 14 TRANSFER ERROR
- 13 MASSBUS CONTROL PARITY ERROR
- 11 DRIVE AVAILABLE

- 10 PORT SELECT
- <09:08> UNIBUS ADDRESS EXTENSION BITS 17 AND 16
- 06 INTERRUPT ENABLE

MR 2599

RH11 – RPDS – Drive Status

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
076712 (MB-01)	ATTN ERROR	PIP	MOL	WRITE LOCK	LAST SECT	PROG ABLE	DRIVE PRES	DRIVE READY	VALID VOL	D-1	D>64	GOREV	DIGB	DF20	DF06

NOTE: ALL BITS READ ONLY.

- 15 ATTENTION ACTIVE
- 13 POSITIONING IN PROGRESS
- 12 MEDIUM ON LINE
- 10 LAST SECTOR TRANSFERRED
- 09 PROGRAMMABLE
- 08 DRIVE PRESENT
- 06 VALID VOLUME

- 05 RP04 – DIFFERENCE EQUALS ONE
- 04 RP04 – DIFFERENCE LESS THAN 64
- 03 RP04 – GO REVERSE
- 02 RP04 – DRIVE TO INNER GUARD BAND
- 01 RP04 – DRIVE FORWARD 20 INCH/SEC
- 00 RP04 – DRIVE FORWARD 5 INCH/SEC
- <06:00> RP06 UNUSED

MR 2600

RH11 - RPER1 - Error Register 1

15	DATA CHECK	14	UNSAFE	13	OPER INC	12	DR T ERROR	11	WR LK ERROR	10	IADR ERROR	09	A OV ERROR	08	H CRC ERROR	07	H COM ERROR	06	ECC ERROR	05	WR CK FAIL	04	FMT ERROR	03	PAR ERROR	02	RMR	01	ILL REG	00	ILL FUNC
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NOTE: ALL BITS READ/WRITE.

- 13 OPERATION INCOMPLETE
- 12 DRIVE TIMING ERROR
- 11 WRITE LOCK ERROR
- 10 INVALID ADDRESS ERROR
- 09 ADDRESS OVERFLOW ERROR
- 08 HEADER CRC ERROR
- 07 HEADER COMPARE ERROR

- 06 ECC HARD ERROR
- 05 WRITE CLOCK FAIL
- 04 FORMAT ERROR
- 03 PARITY ERROR
- 02 REGISTER MODIFICATION REFUSED
- 01 ILLEGAL REGISTER
- 00 ILLEGAL FUNCTION

MR 2601

RH11 - RPMR - Maintenance Register

15		14		13		12		11		10	HI CT DET	09	SBYTE DET	08	ZERO DET	07	DATA ENV	06	ECC ENV	05	MANT WRITE	04	MANT READ	03	MANT SCLK	02	MANT INDEX	01	MANT CLOCK	00	DIAG MODE
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NOTE: ALL BITS READ/WRITE.

- 10 HIGH COUNT DETECT
- 09 SYNC BYTE DETECTED
- 08 ZERO DETECT
- 07 DATA ENVELOPE

- 06 ECC ENVELOPE
- 03 MAINTENANCE SECTOR CLOCK
- 00 DIAGNOSTIC MODE

MR 2602

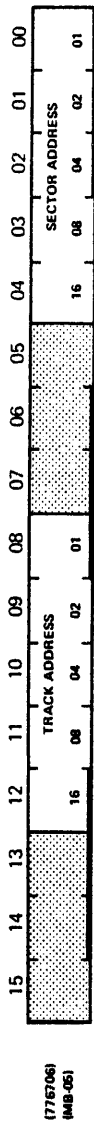
RH11 - RPAS - Attention Summary

15		14		13		12		11		10		09		08		07		06		05		04		03		02		01		00
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NOTE: ALL BITS READ/WRITE.

MR 2603

RH11 - RPDA - Desired Track/Sector Address

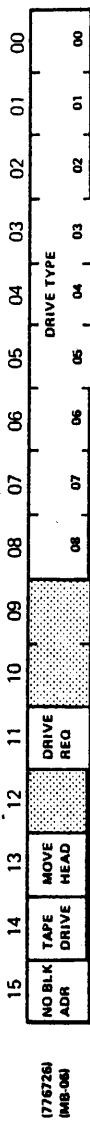


(776706)
(MB-05)

NOTE: ALL BITS READ/WRITE.

MR 2604

RH11 - RPDT - Drive Type



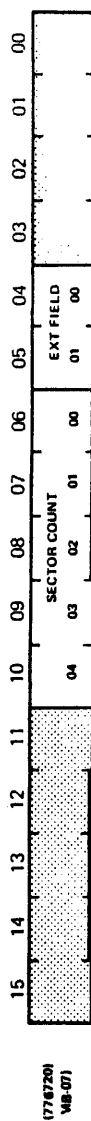
(776726)
(MB-06)

NOTE: ALL BITS READ ONLY.

15 NOT BLOCK ADDRESSED 13 MOVING HEAD
14 TAPE DRIVE 11 DRIVE REQUEST REQUIRED

MR 2605

RH11 - RPLA - Look Ahead



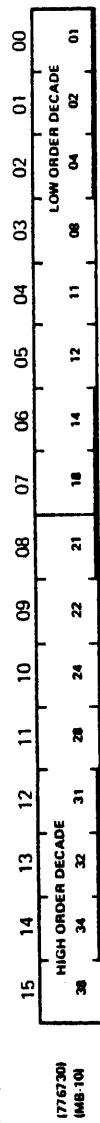
(776720)
(MB-07)

NOTE: ALL BITS READ ONLY.

<05:04> EXTENSION FIELD
05 04 HEAD LOCATION
0 0 - <20% (IN FIRST 20% OF SECTOR)
0 1 - 20 - 40%
1 0 - 40 - 80%
1 1 - >80% (IN LAST 20% OF SECTOR)

MR 2606

RH11 - RFSN - Serial Number



NOTE: ALL BITS READ ONLY.
REFER TO DCL PRINT ECB.

MR-2607

RH11 - RPOF - Offset



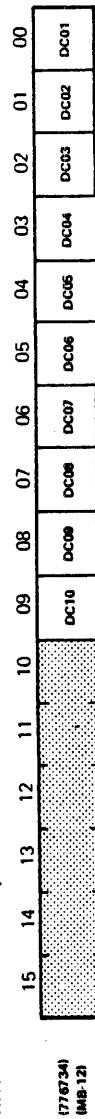
NOTE: ALL BITS READ/WRITE.

15 SIGN CHANGE
12 FORMAT 22 SECTORS

11 ECC INHIBIT
10 HEADER COMPARE INHIBIT

MR-2608

RH11 - RPDC - Desired Cylinder



NOTE: ALL BITS READ WRITE.

MR-2610

RH11 - RPEC1 - ECC Position Register

(776744) (M8-16)	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
				4096	2048	1024	512	256	128	64	32	16	8	4	2	1
				ECC ERROR LOCATION												

NOTE: ALL BITS READ ONLY.

<12:00> BURST LOCATION CODE FOR ECC

MR 2613

RH11 - RPEC2 - ECC Pattern

(776746) (M8-17)	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
						10	09	08	07	06	05	04	03	02	01	00
						ECC MASK BITS										

NOTE: ALL BITS READ ONLY.

<10:00> ERROR BURST AT COMPLETION OF ECC

MR 2614

MTCS1 -- Control Register 1

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SPECL COND	XFER ERROR	MASSB PE		DRIVE AVAIL	PORT SEL	A 17	A 16	READY	INT ENB	05	04	03	02	01	GO

(772440)
(MB-00)

NOTE: ALL BITS READ/WRITE.

- 15 SPECIAL CONDITION
- 14 TRANSFER ERROR
- 13 MASSBUS CONTROL BUS PARITY ERROR
- 11 DRIVE AVAILABLE

- 10 PORT SELECT ADDRESS 17-16
- 06 <09-08> INTERRUPT ENABLE

MR 2615

MTDS -- Status Register

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATTN ACT	COMP ERROR	PIP	MOL	WRITE LOCK	EOT		DRIVE PRES	DRIVE READY	SLAVE STAT	PHASE STAT	SET DOWN	IDB DECT	TAPE MARK	BOT	SLAVE ATTN

(772462)
(MB-01)

NOTE: ALL BITS READ ONLY

- 15 ATTENTION ACTIVE
- 14 COMPOSITE ERROR
- 13 POSITIONING IN PROGRESS
- 12 MEDIUM ON LINE
- 10 END OF TAPE
- 08 DRIVE PRESENT

- 06 SLAVE STATUS CHANGE
- 05 PHASE ENCODED STATUS
- 04 SETTLE DOWN
- 03 IDENTIFICATION BURST DETECTED
- 02 TAPE MARK DETECTED
- 01 BEGINNING OF TAPE
- 00 SLAVE ATTENTION

MR 2620

MTER -- Error Register

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CORR CRC	UN SAFE	OPER INC	DRT ERROR	NXF	CS ITM	FC ERROR	NSTD GAP	PFE LRC	NDE VPE	D BUS PE	FMT ERROR	CBUS PE	REG MOD	ILL REG	ILL FUNC

(772464)
(MB-02)

NOTE: ALL BITS READ ONLY

- 15 CORRECTABLE DATA ERROR OR CRC READ DOES NOT MATCH COMPUTED CRC
- 14 UNSAFE
- 13 OPERATION INCOMPLETE
- 12 DRIVE TIMING ERROR
- 11 NONEXECUTABLE FUNCTION
- 10 CORRECTABLE SKEW OR ILLEGAL TAPE MARK (NRZI)
- 09 FRAME COUNT ERROR
- 08 NONSTANDARD GAP TAPE CHAR
- 07 PE-FORMAT ERROR OR NRZI CHECK CHART ERROR
- 06 PE-NONCORRECTABLE DATA ERROR
- 05 NRZI - VERTICAL PARITY ERROR
- 04 DATA BUS PARITY ERROR
- 03 FORMAT ERROR
- 02 CONTROL BUS PARITY
- 01 REGISTER MODIFICATION REFUSED
- 00 ILLEGAL REGISTER

MR 2621

MTMR -- Maintenance Register

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
08	07	MAINTENANCE DATA FIELD						SEL SCLK	MAINT CLK	MAIN OP CODE			MAINT MODE		

(772464)
(MB-03)

NOTE: ALL BITS READ/WRITE.

- 06 SELECTED SLAVE CLOCK: WRT
- 05 CLOCK SIG GEN BY SEL SLAVE
- 04 MAINTENANCE CLOCK
- 03 <04-01> MAINTENANCE OPERATION CODE
- 02 MAINTENANCE MODE

MR 2626

MTAS -- Attention Summary

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
								ATTENTION SUMMARY							

(772464)
(MB-04)

NOTE: ALL BITS READ/WRITE

MR 2622

MTFC -- Frame Count

(772468) (MB-05)	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

NOTE: ALL BITS READ/WRITE

MR 2618

MTDT -- Drive Type

(772468) (MB-08)	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
	NSA	TAPE DRIVE	MOVE HEAD	7 CH	DRIVE REQ	SLAVE PRES		08	07	06	05	04	03	02	01	00	
									DRIVE TYPE (011 - 1016) (012 - TU48)								

NOTE: ALL BITS READ ONLY

- 15 NOT SECTOR ADDRESSED
- 14 TAPE DRIVE
- 13 NONMOVING HEAD UNIT
- 12 7 CHANNEL UNIT - NEGATED ON
- 11 DRIVE REQUEST REQUIRED
- 10 SLAVE PRESENT
- 9 CHANNEL DRIVE OR POWER LOSS

MR 2627

MTCK - Check Character



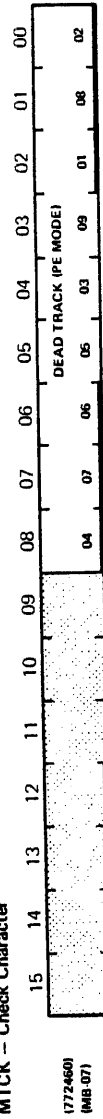
(772460)
(MB-07)

NOTE: ALL BITS READ ONLY

08 CONTROL BUS PARITY

MR 2623

MTCK - Check Character

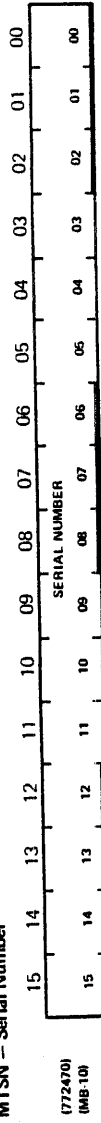


(772460)
(MB-07)

NOTE: ALL BITS READ ONLY

MR 2624

MTSN - Serial Number



(772470)
(MB-10)

NOTE: ALL BITS READ ONLY

MR 2628

MTTC -- Tape Control

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(772472) (MR-11)	ACCL STAT	FRAME TAPE WRITE	EAD DTE		DENSITY 02 01			FORMAT SELECT 03 02 01 00		EVEN PAR 00		SLAVE SEL 02 01 00			

NOTE: ALL BITS READ/WRITE

- 15 ACCELERATION 12 ENABLE ABORT ON DATA TRANSFER ERROR
- 14 FRAME COUNT STATUS 03 EVEN PARITY
- 13 TAPE CONTROL WRITE

MR 2629

MTBA -- Unibus Address

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(772444)															

NOTE: ALL BITS READ/WRITE

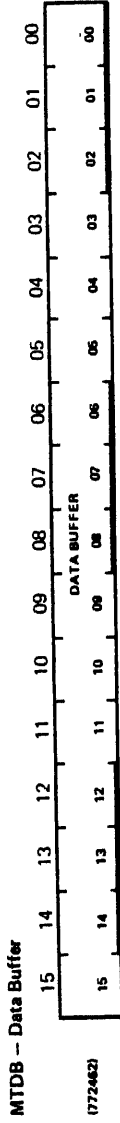
MR 2617

MTCS2 -- Control Register 2

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(772450)	DATA LATE	WRITE CHECK	PAR ERROR	NO DRIVE	MEM ERROR	PGM XFER	MISED BUSPE	DATA BUSPE	OUT READY	IN READY	CONT CLEAR	PAR TEST	BA INC	UNIT SELECT	

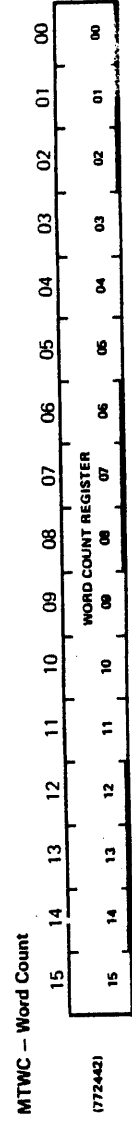
- 14 WRITE CHECK ERROR 08 MASSBUS DATA BUS PARITY ERROR
- 13 PARITY ERROR 07 OUTPUT READY
- 12 NONEXISTENT DRIVE 06 INPUT READY
- 11 NONEXISTENT MEMORY 05 CONTROLLER CLEAR
- 10 PROGRAM ERROR 04 PARITY TEST
- 09 MISSED TRANSFER 03 BUS ADDRESS INCREMENT INHIBIT
- 08 MASSBUS DATA BUS PARITY ERROR

MR 2619



NOTE: ALL BITS READ/WRITE

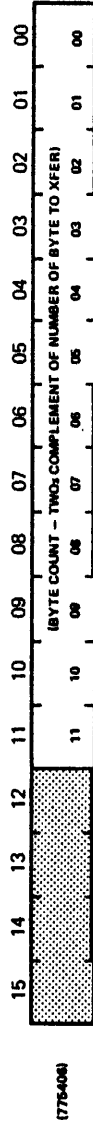
MR 2625



NOTE: ALL BITS READ/WRITE

MR 2616

LPBCTR – DMA Byte Count Register

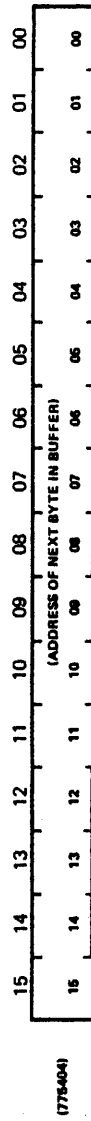


(776404)

NOTE: ALL BITS READ/WRITE.

MR-2015

LPBSAD – DMA Bus Address Register

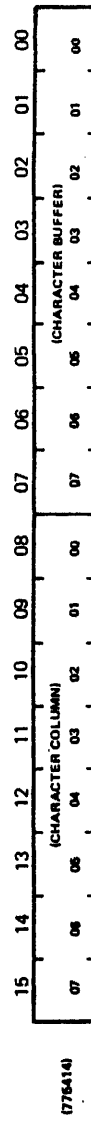


(776404)

NOTE: ALL BITS READ/WRITE

MR-2014

LPCTR – Column Count Register (High Byte)
 LPCBUF – Character Buffer Register (Low Byte)



(776414)

NOTE: BITS <15:08> READ/WRITE

MR-2018

LPCSRB -- Control and Status Register "g"

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VALID DATA	LA180	NOT RDY	PAR BIT	OP VFU	R/W	R/W	(TEST)	OFF LINE	VFU ERROR	PAR ERROR	MEM ERROR	RAM ERROR	SYNC TO	DEM TO	GO ERROR
R	R	R	R	R	R/W	R/W	00	R	R	R	R	R	R	R	R/W

14	SET IF LA180 TYPE PRINTER	FORCE ERROR CONDITIONS
13	NOT READY (OTHER THAN TAPE FAULT)	02 01 00
12	DATA PARITY BIT (AS SENT TO PRINTER)	0 0 0
11	OPTICAL VFU (ZERO IF DAVFU)	0 0 1
06	PARITY ERROR AT PRINTER	0 1 0
04	MEMORY PARITY ERROR	0 1 1
03	RAM PARITY ERROR DURING DMA XFER	1 0 0
02	MASTER SYNC TIME OUT (NO SYNC)	1 0 1
01	DEMAND TIME OUT	1 1 0
00	GO SET AND "ERROR" OR "DEMAND	1 1 1

MR-2016

LPPCTR -- Page Count Register

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00							
											PAGE COUNT											
											11	10	09	08	07	06	05	04	03	02	01	00

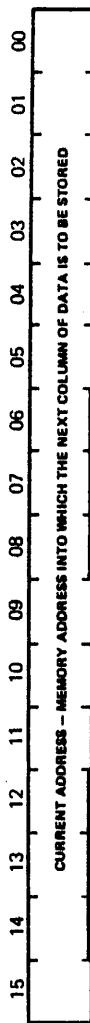
(776410)

NOTE: ALL USED BITS READ/WRITE

MR-2017

CDBA - Current Address Register

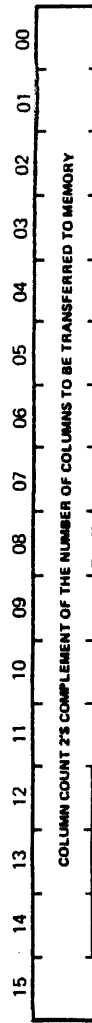
(777164)



MR 2632

CDCC - Column Count Register

(777163)



MR 2627

CDDB -- Data Buffer Register -- Nonpacking Mode

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ZONE 12		ZONE 11		ZONE 10		ZONE 09		ZONE 08		ZONE 07		ZONE 06		ZONE 05	
ZONE 12		ZONE 11		ZONE 10		ZONE 09		ZONE 08		ZONE 07		ZONE 06		ZONE 05	

(7771661)

MR 2633

CDDB -- Data Buffer Register -- Packing Mode

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ZONE 12		ZONE 11		ZONE 10		ZONE 09		ZONE 08		ZONE 07		ZONE 06		OCTAL CODE ZONES 1-7	
ZONE 12		ZONE 11		ZONE 10		ZONE 09		ZONE 08		ZONE 07		ZONE 06		OCTAL CODE ZONES 1-7	

(7771661)

MR 2634

CDST -- Status and Control Register

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ERROR CHECK	READR CHECK	END. FILE	OFF LINE	DATA ERROR	DATA LATE	NO. MEM	POWER CLEAR	READY	INTER ENB	HOPPER CHECK		TRANS LINE	HOPPER CHECK	DATA PACK	READ
06	08	13	14	11	10	09	08	07	06	05	04	03	02	01	00
06	08	13	14	11	10	09	08	07	06	05	04	03	02	01	00

(7771901)

MR 2630

PARCSR — Parameter Control and Status Register

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WRITE (76XXX2)	DEC MODE	SEC MODE	SEC MODE	SEC MODE	CRC INHIB	CRC INHIB	SECONDARY STATION ADDRESS	RECEIVER SYNC	RECEIVER SYNC	RECEIVER SYNC	RECEIVER SYNC	RECEIVER SYNC	RECEIVER SYNC	RECEIVER SYNC	RECEIVER SYNC

NOTE: XXX = 030 (DUP 0), 031 (DUP 1)

12 SECONDARY MODE SELECT

09 CRC INHIBIT

MR 2637

RXCSR — Receiver Control and Status Register

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DATA SET A	RING SEND	CLEAR SEND	CAR- RIER	RX ACTIVE	SECRX DATA	DATA READY	STRIP SYNC	RX DONE	RX INTEN	DATA INTEN	RX ENB	SECTX DATA	REQ SEND	TERM RDY	DATA SET B

NOTE: XXX = 030 (DUP 0), 031 (DUP 1)

- 15 DATA SET CHANGE A
- 13 CLEAR TO SEND
- 11 RECEIVER ACTIVER
- 10 SECONDARY RECEIVED DATA
- 09 DATA SET READY
- 07 RECEIVER DONE

- 06 RECEIVER INTERRUPT ENABLE
- 05 DATA SET INTERRUPT ENABLE
- 04 RECEIVER ENABLE
- 03 SECONDARY TRANSMIT DATA
- 02 REQUEST TO SEND
- 01 DATA TERMINAL READY
- 00 DATA SET CHANGE B

MR 2635

RXDBUF — Receiver Data Buffer Register

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
READ (76XXX2)	RX ERR	RX OVRUN	RXCRC ERR	RXCRC ERR	RX ABORT	RXEND MSG	START MSG	RECEIVE DATA	RECEIVE DATA	RECEIVE DATA	RECEIVE DATA	RECEIVE DATA	RECEIVE DATA	RECEIVE DATA	RECEIVE DATA

NOTE: XXX = 030 (DUP 0), 031 (DUP 1)

- 15 RECEIVER ERROR
- 14 RECEIVER OVERRUN
- 12 RECEIVER CRC ERROR

- 10 RECEIVER ABORT
- 09 END OF RECEIVED MESSAGE
- 08 START OF RECEIVED MESSAGE

MR 2636

TXCSR - Transmitter Control and Status Register

15	DATA LATE	R	14	MAINT OUT	R/W	13	MAINT CLK	R/W	12	MAINT MODEA	R/W	11	MAINT MODEB	R/W	10	MAINT IN	R/W	09	TX ACT	R	08	DEVICE RESET	W	07	TX DONE	R	06	TX INTEN	R/W	05	SEND	R/W	04	HALF DUP	R/W	03	02	01	00
----	-----------	---	----	-----------	-----	----	-----------	-----	----	-------------	-----	----	-------------	-----	----	----------	-----	----	--------	---	----	--------------	---	----	---------	---	----	----------	-----	----	------	-----	----	----------	-----	----	----	----	----

(76XXX4)

NOTE: XXX - 030 (DUP 0), 031 (DUP 1)

- 15 TRANSMITTER DATA LATE ERROR
- 14 MAINTENANCE TRANSMIT DATA OUT
- 13 MAINTENANCE CLOCK
- 12 MAINTENANCE MODE SELECT A
- 11 MAINTENANCE MODE SELECT B
- 10 MAINTENANCE INPUT DATA
- 09 TRANSMITTER ACTIVE
- 08 DEVICE RESET
- 07 TRANSMITTER DONE
- 06 TRANSMITTER INTERRUPT ENABLE
- 05 HALF DUPLEX FULL DUPLEX

MR 2638

TXDBUF - Transmitter Data Buffer Register

15	DATA	R/W	14	START MSG	R/W	13	END MSG	R/W	12	TXCRC IN	R	11	MAINT TX ABORT	R/W	10	TXCRC IN	R	09	TXCRC IN	R	08	TXCRC IN	R	07	TXCRC IN	R	06	TXCRC IN	R	05	TXCRC IN	R	04	TXCRC IN	R	03	TXCRC IN	R	02	TXCRC IN	R	01	00
----	------	-----	----	-----------	-----	----	---------	-----	----	----------	---	----	----------------	-----	----	----------	---	----	----------	---	----	----------	---	----	----------	---	----	----------	---	----	----------	---	----	----------	---	----	----------	---	----	----------	---	----	----

(76XXX6)

- 14 RECEIVER CRC INTERNAL
- 13 TRANSMITTER CRC INTERNAL
- 12 MAINTENANCE TIMER
- 11 TRANSMITTER DATA LATE ERROR
- 10 TRANSMITTER DATA OUT
- 09 MAINTENANCE TRANSMIT DATA OUT
- 08 MAINTENANCE CLOCK
- 07 MAINTENANCE MODE SELECT A
- 06 MAINTENANCE MODE SELECT B
- 05 TRANSMITTER INTERRUPT ENABLE
- 04 HALF DUPLEX FULL DUPLEX
- 03 TRANSMITTER DONE
- 02 TRANSMITTER ACTIVE
- 01 MAINTENANCE INPUT DATA
- 00 DEVICE RESET

MR 2639

CSR - Control and Status Register

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
XMTR READY (7600XX)	XMTR INTER WORDS	SILO ALARM	XMTR 4	LINE 2	BITS 1	RCVR DONE	RCVR INTER	LINE SCAN	CLEAR CSR	MAINT LOOP					

NOTE: XX = 10 (DZ 0), 20 (DZ 1), 30 (DZ 2), 40 (DZ 3)

- 15 TRANSMIT READY 07 RECEIVER DONE
- 14 TRANSMIT INTERRUPT ENABLE 06 RECEIVER INTERRUPT
- 13 SILO HAS 16 WORDS 05 TURN ON LINE SCAN
- 12 SILO ALARM INTERRUPT WHEN BIT 13 ON 04 CLEAR UARTS, SILO, CSR, 15 MS LONG
- <10:08> TRANSMIT LINE BITS 03 MAINTAIN LOOP TRANSMIT TO RECEIVE

MR 2642

CSR - Control and Status Register

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
XMTR INTER	SILO ALARM	RCVR INTER	LINE SCAN	CLEAR CSR	MAINT LOOP										

NOTE: XX = 10 (DZ 0), 20 (DZ 1), 30 (DZ 2), 40 (DZ 3)

- 14 TRANSMIT INTERRUPT ENABLE 05 TURN ON LINE SCAN
- 12 ENABLE SILO ALARM INTERRUPT 04 CLEAR UARTS, SILO, CSR
- 06 RECEIVE INTERRUPT ENABLE 03 MAINTAIN LOOP TRANSMIT TO RECEIVE

MR 2641

TCR - Transmit Control Register

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DTR TO MODEM LINES								TRANSMIT ENABLE LINES							
07	06	05	04	03	02	01	00	07	06	05	04	03	02	01	00

NOTE: XX = 14 (DZ 0), 24 (DZ 1), 34 (DZ 2), 44 (DZ 3)

MR 2646

TCR - Transmit Control Register

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DTR TO MODEM LINES								TRANSMIT ENABLE LINES							
07	06	05	04	03	02	01	00	07	06	05	04	03	02	01	00

NOTE: XX = 14 (DZ 0), 24 (DZ 1), 34 (DZ 2), 44 (DZ 3)

MH 2645

TDR - Transmit Data Register

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BREAK LINES								TRANSMIT DATA BITS							
07	06	05	04	03	02	01	00	07	06	05	04	03	02	01	00

NOTE: XX = 16 (DZ 0), 26 (DZ 1), 36 (DZ 2), 46 (DZ 3)

MH 2647

KMC - BSEL 1 - Maintenance Register

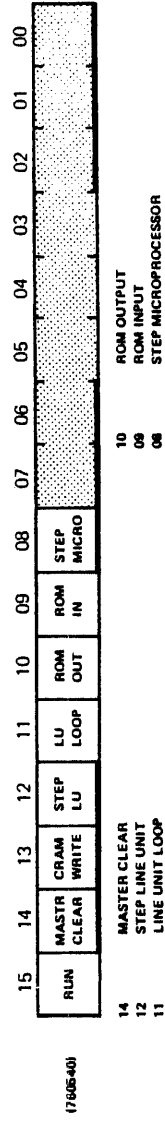


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CHECKS/ADJ.

NOTES

UNIBUS ADAPTER MINI CHECK

If you are having problems booting from either your disk or magtape, try this Unibus wraparound test.

```

EI UBA#,763000          ;ADDRESS OF PAGING RAM FOR LOCATION
                        ZERO
DI 40000 (18 BIT VALID),140000 (36 BIT,VALID),240000
                        (16 BIT,VALID)
EI UBA#,763101          ;ADDRESS OF UBA MAINTENANCE REGISTER
DI 1                    ;BIT 35 FOR WRAP AROUND
EI UBA#,ADR             ;LOAD MEMORY ADDRESS TO BE WRITTEN
                        ;LOW ORDER UNIBUS ADDRESS BITS ARE DISCARDED
                        ;C00 SAYS 8 BIT UNIBUS BYTE MODE OR NOT
                        ;C01 SAYS RIGHT HALF OR LEFT HALF

                        3,,0=LH MEMORY LOCATION 0
                        3,,2=RH MEMORY LOCATION 0
                        3,,4=LH MEMORY LOCATION 1
                        3,,6=RH MEMORY LOCATION 1
DI XXXXXX(DATA PATTERN) ;DATA WILL LOOP THROUGH UBA TO
EM MEMORY LOCATION      ;CHECK TO SEE IF IT GOT THERE

```

```

EXAMPLE 1:  EI 1763000
            DI 140000
            EI 1763101
            DI 1
            EI 1000100
            EI 555333
            DI 1000102
            DI 121212
            EM 20
CORRECT DATA SHOULD BE 000000,,000020/555333,,121212

```

```

EXAMPLE 2:  EI 1763000
            DI 40000
            EI 1763101
            DI 1
            EI 1000100
            DI 777777
            EM 20
CORRECT DATA SHOULD BE 000000,,000020/777777,,000020

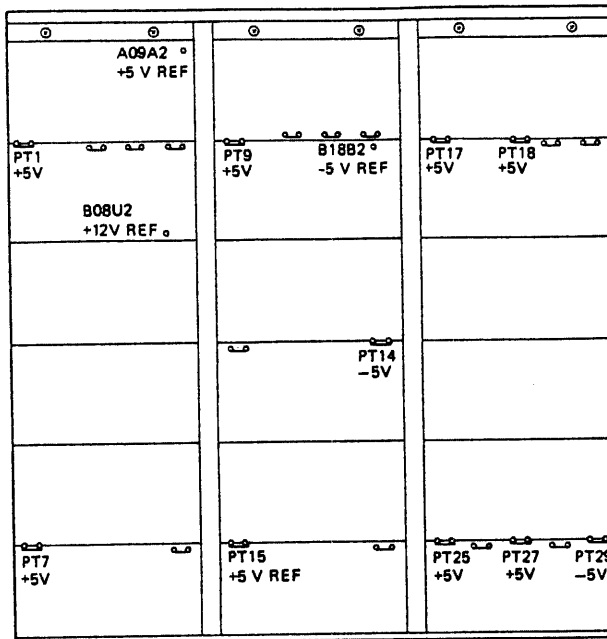
```

```

EXAMPLE 3:  EI 1763000
            DI 240000
            EI 1763101
            DI 1
            EI 1000100
            DI 743216
            EM 20
CORRECT DATA SHOULD BE 000000,,000020/143216,,000020

```

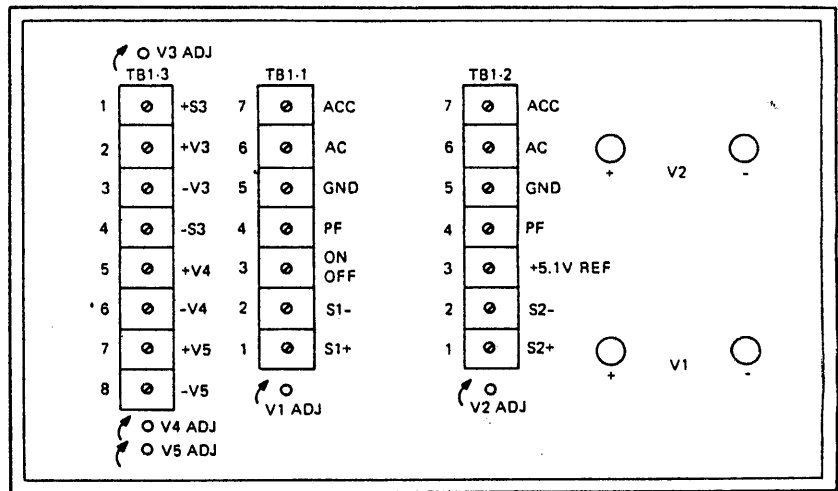
CHECKS/ADJ.



PIN	REFERENCE	ADJUSTMENT	
A09A2	+5 V REF	ADJ V1	ADJUSTMENTS MADE ON LH POWER SUPPLY
B08U2	+12 V REF	ADJ V3	
B18B2	-5 V REF	ADJ V5	
PT 15	+5 V REF	ADJ V2	

KS10 BACKPLANE

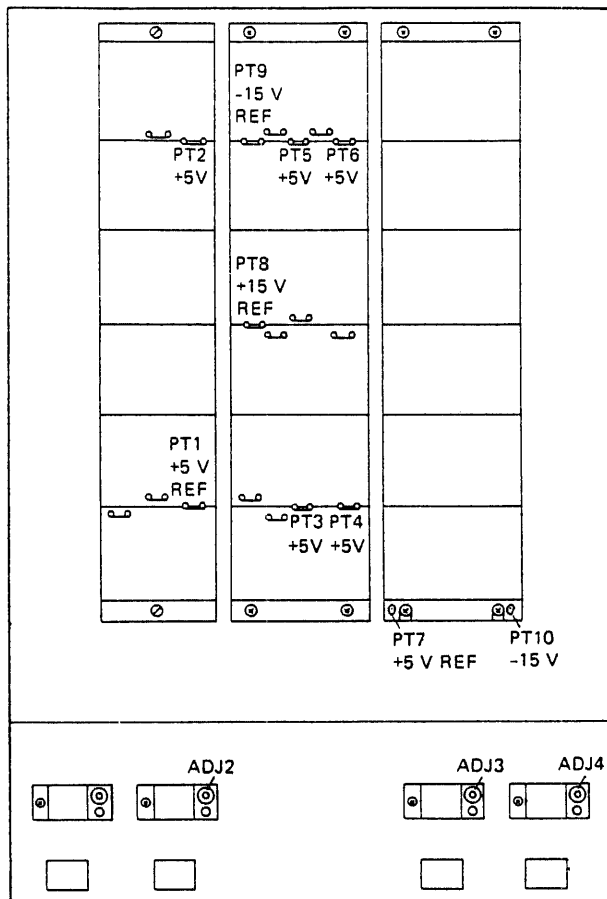
MR-2708



H7130 POWER SUPPLY

MR 1916

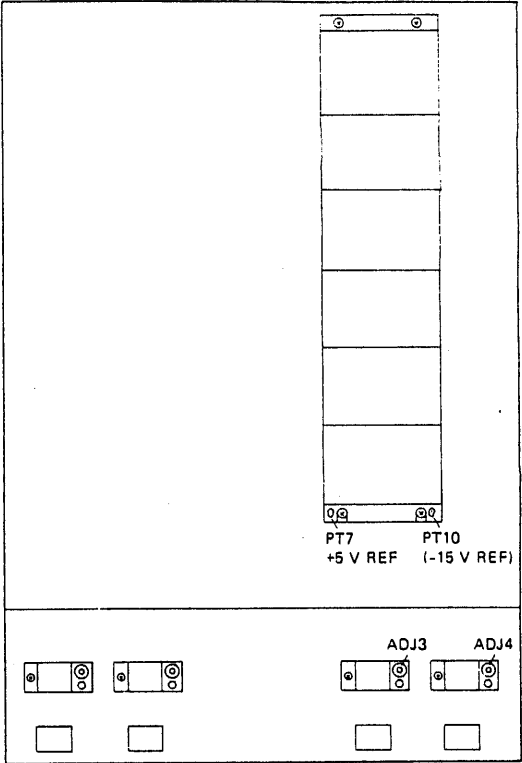
CHECKS/ADJ.



PIN	REFERENCE	ADJUSTMENT
PT1	+5 V REF	ADJ2
PT7	+5 V REF	ADJ3
PT8	+15 V REF	NO ADJ
PT9	-15 V REF	ADJ4

BA11-K BACKPLANE

MR-2707



PIN	REFERENCE	ADJUSTMENT
PT7	+5 V REF	ADJ3
PT10	-15 V REF	ADJ4

MR 3115

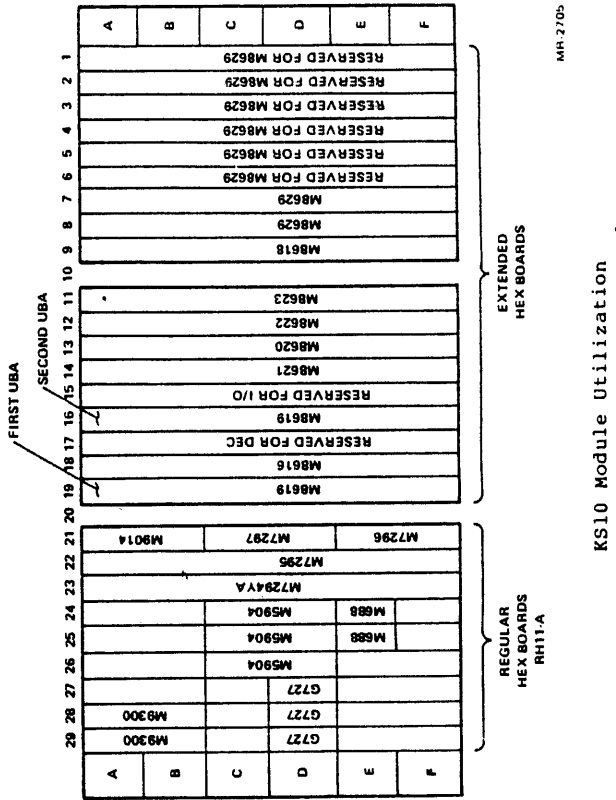
BALL-K Power Tab and Adjustment Locations (DNHXX Cabinet)

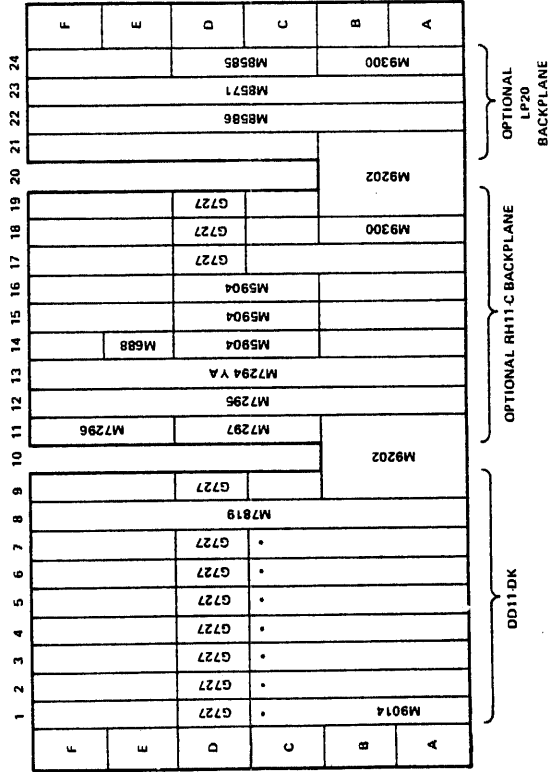
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DIAGRAMS/MULS

NOTES





OPTION VARIATIONS*

SLOTS	ASYNC LINES 8-15	ASYNC LINES 16-23	ASYNC LINES 24-32
2			
3			
4			
5			M7819 DZ11
6	M7819 DZ11		
7	M7819 STD		
8			

SLOTS	1ST SYNC	2ND SYNC
2	M8204 KMC11	
3		M7867 DUP11
4	M7867 DUP11	
5		
6		
7		
8		

MH 7/06

Ball-K Module Utilization (Module Side)

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STANDARD BOOT PROCEDURE

The KS10 is automatically booted 30 seconds after power-up. Booting may also be accomplished by the console BT command.

PRE-BOOT Error Messages

PRE-BOOT is loaded from disk or magtape (see 8080 commands DS, MS, BT, BT1, MT, MT1).

PRE-BOOT is written onto the disk using "SMFILE.EXE". It also is written on "standard" diagnostic tapes and onto the "Monitor Distribution" tapes.

PRE-BOOT is loaded by the 8080 into memory locations 1000 and up, and starts at 1000. The ERROR halts are:

1001 Found "bad" core-transfer address (page 1 is illegal -- can't overload PRE-BOOT)

1002 Disk retry error or magtape read error

1003 No RH11 base address

1004 Magtape skip failure

At ERROR halt time the following memory locations contain the following information.

Location	Disk Booting	Magtape Booting
100	8080 disk address	Not used
101	Memory transfer address	same
102	T3, selection pickup pointer	same
103	RPCS1-register	MTCS1-register
104	RPCS2-register	MTCS2-register
105	RPDS - register	MTDS -- register
106	RPER1-register	MTER1-register
107	RPER2-register (RP06 only)	Not used
110	RPER3-register	Not used
111	UBA Page RAM loc 0	same
112	UBA-status register	same
113	Version Nr of PRE-BOOT	same

NOTE

The 8080 disk address is in the form "CY SA TA".

DIAGNOSTIC PROGRAM HIERARCHIES

The following tables describe the 10-Based 10 Maintenance Library diagnostic hierarchies.

Table 1 KS10 Maintenance Library Utility Programs

Table 2 KS10 Processor Diagnostic Hierarchy

Table 3 KS10 Memory Diagnostic Hierarchy

Table 4 Disk Subsystems Diagnostic Hierarchy

Table 5 Magtape Subsystems Diagnostic Hierarchy

Table 6 Hardcopy Equipment Diagnostics

Table 7 Communications Equipment Diagnostics

Table 8 Unibus Adapter Diagnostic

Table 9 Miscellaneous Diagnostic

MODE:

E indicates that the program may be run in Executive mode.

U indicates that the program may be run in the User mode.

Table 1 KS10 Maintenance Library Utility Programs

Utility	Mode	Title
SMAPT.SAV	E	Special Program
SMBC2.SAV	E U	KS10 Boot Check 2
SMDDT.SAV	E U	KS10 DDT
SMFILE.EXE	U	Special Program
SMMAG.SAV	E U	KS10 Magtape Monitor
SMMON.SAV	E U	KS10 Diagnostic Monitor
		SMCPU Processor Diagnostics Run File
		SMFLT Processor Diagnostics Run File (FLT)
		SMUSR Processor Diagnostics Run File (TS)
SMTAPE.SAV		Magtape Creator
SUBSM.SAV	E	KS10 Executive Subroutine Program
SUBUSR.SAV	U	KS10 User Subroutine Program

Table 2 KS10 Processor Diagnostic Hierarchy

Diagnostic	Mode	Title
Basic, Advanced, and Reliability		
DSKAA.SAV	E U	Basic Instruction Diagnostic 1
DSKAB.SAV	E U	Basic Instruction Diagnostic 2
DSKAC.SAV	E U	Basic Instruction Diagnostic 3
DSKAD.SAV	E U	Basic Instruction Diagnostic 4
DSKAE.SAV	E U	Basic Instruction Diagnostic 5
DSKAF.SAV	E U	Basic Instruction Diagnostic 6
DSKAG.SAV	E U	Basic Instruction Diagnostic 7
DSKAH.SAV	E	Basic Instruction Diagnostic 8
DSKAI.SAV	E U	Basic Instruction Diagnostic 9
DSKAJ.SAV	E U	Basic Instruction Diagnostic 10
DSKAK.SAV	E U	Basic Instruction Diagnostic 11
DSKAL.SAV	E U	Basic Instruction Diagnostic 12
DSKAM.SAV	E U	Basic Instruction Diagnostic 13
DSKBA.SAV	E U	Basic Instruction Reliability 1
DSKCA.SAV	E U	Advanced Instruction Diagnostic 1
DSKCB.SAV	E U	Advanced Instruction Diagnostic 2
DSKCC.SAV	E U	Advanced Instruction Diagnostic 3
DSKCD.SAV	E U	Advanced Instruction Diagnostic 4
DSKCE.SAV	E U	Advanced Instruction Diagnostic 5
DSKCF.SAV	E U	Advanced Instruction Diagnostic 6
DSKCG.SAV	E U	Advanced Instruction Diagnostic 7
DSKDA.SAV	E U	Arithmetic Reliability
Paging And Cache Tests		
DSKEA.SAV	E	Paging Diagnostic
DSKEB.SAV	E	Cache Diagnostic
Supplementary Tests		
DSKFA.SAV	E	Instruction Timing Diagnostic

Table 3 KS10 Memory Diagnostic Hierarchy

Diagnostic	Mode	Title
DSMMA.SAV	E	Memory Diagnostic
DSMMD.SAV	E U	Memory Diagnostic
Supplementary Tests		
DSMMB.SAV	E U	BLT/FLT I/O Memory Diagnostic
DSMMC.SAV	E U	FAST AC Diagnostic

Table 4 Disk Subsystems Diagnostic Hierarchy

Diagnostic	Mode	Title
DSRMA.SAV	E	RM03 Basic Diagnostic
DSRMB.SAV	E U	RM03/RP06 Reliability
DSRPA.SAV	E	RP06 Basic Diagnostic

Table 5 Magtape Subsystems Diagnostic Hierarchy

Diagnostic	Mode	Title
DSTUA.SAV	E U	RH11 TM03/TU45 Basic Diagnostic
DSTUB.SAV	E U	Magtape Reliability

Table 6 Hardcopy Equipment Diagnostics

Diagnostic	Mode	Title
DSCDA.SAV	E U	Card Reader Diagnostic
DSLPA.SAV	E U	Line Printer Diagnostic
DSLTA.SAV	E U	Teletype Diagnostic

Table 7 Communications Equipment Diagnostics

Diagnostic	Mode	Title
DSDUA.SAV	E	DUP-11 Diagnostic
DSDZA.SAV	E	DZ-11 Diagnostic
DSKMA.SAV	E	KMC-11 Diagnostic

Table 8 Unibus Adapter Diagnostic

Diagnostic	Mode	Title
DSUBA.SAV	E	Unibus Adapter Diagnostic

Table 9 Miscellaneous Diagnostic

Diagnostic	Mode	Title
DSRHH.SAV	E	RH11 TB Diagnostic (manufacturing)

GENERAL INFORMATION

CODE: KNS10
 TITLE: CONSOLE PROGRAM
 ABSTRACT: Console program resides in the 8080 PROMs and supports the KS10 based system. The console operates in either of two modes.

1. User Mode - The CTY is a user terminal and commands are passed to and from the KS10 CPU under control of the console program.
2. Console Mode - Commands are directed to (and executed by) the 8080 console hardware. The console program initialized the CTY-to-console mode at power-up.

NOTE: NONE

LOADING AND STARTING PROCEDURE: KS10 is automatically booted 30 seconds after power-up.

OPERATIONAL CONTROL

The KS10 is directed by the commands listed in Table 2.

Table 1 lists standard console messages.

ERROR MESSAGE SUMMARY

Table 3 lists the standard console error messages.

Table 1 Standard Console Messages

Message	Meaning
BT AUTO	Beginning automatic boot procedure after power-up.
BT SW	Beginning boot procedure as a result of BOOT switch being pressed (LOCK switch in UNLOCK position).
BUS 0-35	Message header for EB command.
CYC	Cycle type for DB command.
ENABLED	Entering CTY mode from user mode. (CTY mode is entered as a result of a "control-\\" in user mode with LOCK switch in UNLOCK position.)
HLTD	Halt in KS10 processor program execution.
KS10>	Command prompt.
OFF	Current state is off. (Response to CE, TE, TP, and KL commands when current state of enable is requested and it is a 0.)
ON	Current state is on. (Response to CE, TE, TP, and KL commands when current state of enable is requested and it is a 1.)
RCVD	Data received from bus. (Indicates bus data received if failure occurred during EB command.)
SENT	Data sent to bus. (Indicates bus data transmitted if failure detected during DB command.)
USR MOD	Entering user mode. (User mode is entered as a result of a "control-2" or the successful completion of a CO, ST, BT, or MT command.)
>>UBA?	Query for UBA number.
>>UNIT?	Query for unit number.
>>TCU	Query for tape controller unit number.
>>RHBASE?	Query for RH11 base register address.
>>DENS?	Query for tape density.
>>SLV?	Query for tape slave number.

Table 2 Console Commands

Command	Description	Notes																				
Special Control Characters																						
^\ ^\\	Enter console mode. Used in conjunction with the KL1 command for KLINIK mode.	NA NA																				
^U	Rub out current line.	NA																				
^O	Switch: first one stops CTY output, second one resumes CTY output.	NA																				
^S	Stop TTY output and 8080 waits for control Q.	NA																				
^Q	Resumes TTY output.	NA																				
^C	Stop the 8080.	NA																				
^Z	Enter User mode.	NA																				
RUB-OUT	Rub out previous character typed.	NA																				
Load Commands																						
LAXx	LAXx <CR> - Set KS10 memory address xx (0000000-1777777).	NA																				
LCxx	LCxx <CR> - Set CRAM address xx (0000-3777).	NA																				
LFxx	LFxx <CR> - Load diagnostic write function xx (0-7). The function specifies a 12-bit group within a CRAM address. <table border="1"> <thead> <tr> <th>LF</th> <th>CRAM</th> <th>LF</th> <th>CRAM</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>00-11</td> <td>4</td> <td>48-59</td> </tr> <tr> <td>1</td> <td>12-23</td> <td>5</td> <td>60-71</td> </tr> <tr> <td>2</td> <td>24-35</td> <td>6</td> <td>72-83</td> </tr> <tr> <td>3</td> <td>36-47</td> <td>7</td> <td>84-95</td> </tr> </tbody> </table>	LF	CRAM	LF	CRAM	0	00-11	4	48-59	1	12-23	5	60-71	2	24-35	6	72-83	3	36-47	7	84-95	NA
LF	CRAM	LF	CRAM																			
0	00-11	4	48-59																			
1	12-23	5	60-71																			
2	24-35	6	72-83																			
3	36-47	7	84-95																			
LIxx	LIxx <CR> - Set I/O address xx	1																				
LKxx	LKxx <CR> - Set 8080 memory address xx (PROM address = 00000-17777; RAM address = 20000-21777).	NA																				
Deposit Commands																						
DBxx	DBxx <CR> - Deposit xx (36 bits) onto KS10 bus.	NA																				
DCxx	DCxx <CR> - Deposit xx (96 bits) into CRAM. Address previously loaded by LC command.	NA																				
DFxx	DFxx <CR> - Deposit xx (12-bit group) into CRAM Address and diagnostic function previously loaded by LC and LF commands.	NA																				
DIxx	DIxx <CR> - Deposit xx (16, 18 or 36 bits) into an I/O register. Address previously loaded by LI command.	NA																				
DKxx	DKxx <CR> - Deposit xx (8 bits) into 8080 memory. Address previously loaded by LK command (Data cannot be deposited in PROM addresses; only in RAM addresses).	NA																				
DMxx	DMxx <CR> - Deposit xx (36 bits) into KS10 memory. Address previously loaded by LA command or EM.	NA																				
DNxx	DNxx <CR> - Deposit xx into next (KS10, 8080, I/O, CRAM) address.	NA																				

Table 2 Console Commands (Cont)

Command	Description	Notes
Examine Commands		
EB	EB <CR> - Examine KS10 Bus. Prints contents of console registers 100-103 and 300-303.	NA
EC	EC <CR> - Examine contents of CRAM control register.	NA
ECxx	ECxx <CR> - Examine contents of CRAM address xx.	NA
EI	EI <CR> - Examine contents of I/O register. Address previously loaded by LI command.	NA
EIxx	EIxx <CR> - Examine contents of I/O address xx.	NA
EJ	EJ <CR> - Examine current CRAM address, next CRAM address, jump address, and subroutine return address.	NA
EK	EK <CR> - Examine contents of 8080 memory. Address previously loaded by LK command.	NA
EKxx	EKxx <CR> - Examine contents of 8080 memory address xx.	NA
EM	EM <CR> - Examine contents of KS10 memory. Address previously loaded by LA command.	NA
EMxx	EMxx <CR> - Examine contents of KS10 memory address xx.	NA
EN	EN <CR> - Examine contents of next (KS10, 8080, I/O, CRAM) address.	NA
Start/Stop Clock		
CH	CH <CR> - Halt CPU clock.	NA
CP	CP <CR> - Pulse CPU clock.	NA
CPxx	CPxx <CR> - Pulse CPU clock xx times.	NA
CS	CS <CR> - Start CPU clock.	NA
Start/Stop Microcode		
PM	PM <CR> - Pulse microcode. Performs a CP command to execute a microinstruction followed by an EJ command to print current CRAM address, next CRAM address, jump address, and subroutine return address.	NA
SM	SM <CR> - Reset and start microcode at CRAM address 0.	NA
SMxx	SMxx <CR> - Reset and start microcode at CRAM address xx.	NA
TR	TR <CR> - Trace. Repeats PM command until any CTY key is depressed.	NA
TRxx	TRxx <CR> - Trace. Repeats PM command until CRAM address xx is reached or until and CTY key is depressed.	NA

Table 2 Console Commands (Cont)

Command	Description	Notes
Start/Stop Program		
HA	HA <CR> - Halt KS10 program. Microcode enters halt loop.	NA
CO	CO <CR> - Continue KS10 program execution. Console program enters user mode.	NA
SH	SH <CR> - Shut down command. Deposits nonzero data into KS10 memory location 30 to allow orderly shut down of the monitor.	NA
SI	SI <CR> - Single instruct. Executes next KS10 instruction.	NA
STxx	STxx <CR> - Start KS10 program at address xx. Console program enters user mode.	NA
Select Device		
DS	DS <CR> - Select disk for bootstrap or microcode verification. Console program asks for UBA number (default = 1), RH11 base address (default = 776700), and disk unit number (default = 0).	2
MS	MS <CR> - Select tape for bootstrap or for microcode verification. Console program asks for UBA number (default = 3), RH11 base address (default = 772440), tape controller unit number (default = 0), tape density (default = 1600 BPI), and slave number (default = 0).	3
Boot Commands		
BC	BC <CR> - Check the KS10 boot path.	NA
BT	BT <CR> - Bootstrap the KS10 from disk. Loads and starts microcode and monitor boot program from drive 0 on UBA 1 (default address) or drive selected by last DS command; starts KS10 at memory address 1000. The BT command is performed automatically 15 seconds after power-up. A "control C" aborts the automatic boot process.	NA
BT1	Same as BT command except that diagnostic boot program (not monitor boot program) is loaded and started.	
B2	B2 <CR> - Bootcheck 2. This loads in a separate PRE-BOOT which loads in the Bootcheck 2.	NA
LB	LB <CR> - Load the monitor boot program from disk selected last. Does not load microcode. Program must be started at 1000.	NA
LB1	Same as LB command except that diagnostic boot program (not monitor boot program) is loaded. Program must be started at 1000.	
MB	MB <CR> - Load the monitor boot program from the tape selected last. Does not load microcode. Program must be started at 1000.	NA
MT	MT <CR> - Bootstrap the KS10 from tape. Loads and starts microcode and monitor boot program from tape unit 0, slave unit 0 on UBA 3 (default address) or drive selected by last MS command; starts KS10 at memory address 1000.	NA

Table 2 Console Commands (Cont)

Command	Description	Notes
Verify Microcode		
VD	VD <CR> - Verify CRAM against disk. Compares microcode in CRAM with microcode found on disk unit 0 on UBA 1 (default address) or disk selected by last DS command.	NA
VT	VT <CR> - Verify CRAM against tape. Compares microcode in CRAM with microcode found on tape unit 0, slave unit 0 on UBA 3 (default address) or tape selected by last MS command.	NA
Mark/Unmark Microcode		
MKxx	MKxx <CR> - Mark microcode word (set bit 95) at CRAM address xx.	NA
UMxx	UMxx <CR> - Unmark microcode word (clear bit 95) at CRAM address XX.	NA
Master Reset		
MR	MR <CR> - Master reset. Issue bus reset.	NA
Execute Command		
EXxx	EXxx <CR> - Execute the single KS10 systems - level instruction xx.	NA
Enable/Disable		
CExx	CExx <CR> - Enable (xx = 1) or disable (xx = 0) cache.	NA
PExx	PExx <CR> - Enable or disable parity detection as follows. xx 0 Disable all parity detection 4 Enable KS10 bus parity detection 5 Enable DPE/DPM parity detection 6 Enable CRA/CRM parity detection 7 Enable all parity detection	NA
TExx	TExx <CR> - Enable (xx = 1) or disable (xx = 0) CPU interval timer interrupts.	NA
TPxx	TPxx <CR> - Enable (xx = 1) or disable (xx = 0) CPU traps. Following an enable/disable command with a carriage return gives the current value.	NA
SCxx	SCxx <CR> - Enable (xx = 1) or disable (xx = 0) automatic recovery from soft CRAM parity errors.	NA
Read Cram		
RC	RC <CR> - Read CRAM data. Performs diagnostic read functions 0-17 to read CRAM addresses and contents (of current address) as follows. 0 CRAM bits 00-11 10 Parity bits A-F 1 Next CRAM address 11 KS10 Bus bits 24-35 2 CRAM subroutine 12 CRAM bits 36-47 return address (Copy A) 3 Current CRAM address 13 CRAM bits 36-47 (Copy B) 4 CRAM bits 12-23 14 CRAM bits 48-59 5 CRAM bits 24-35 15 CRAM bits 60-71 (Copy A) 6 CRAM bits 24-35 16 CRAM bits 72-3 (Copy B) 7 0's 17 CRAM bits 84-95	NA

Table 2 Console Commands (Cont)

Command	Description	Notes
Zero Memory		
ZM	ZM <CR> - Zero memory. Deposit 0's into all KS10 memory locations.	NA
Repeat Command		
RP	RP <CR> - Repeat last command, or last command string, until any CTY key is depressed.	NA
RPxx	RPxx <CR> - Repeat last command, or last command string, xx times.	NA
Lamp Test		
LT	LT <CR> - Lamp test. Momentarily lights (1-2 seconds) and turns off (1-2 seconds) STATE, FAULT, and REMOTE indicators. The indicators are then returned to their original state.	NA
Password Command		
PWxx	PWxx <CR> - Set password xx (xx = maximum of 6 alphanumeric characters). Following a PW command with a carriage return clears the password storage area.	NA
Klinik Command		
KLxx	KLxx <CR> - Enable remote link with access to system to operate in mode 2 but not in mode 3 (xx = 0). Enable remote link with access to system to operate in mode 2 or in mode 3 (xx = 1). Following a KL command with a carriage return gives the current value.	NA
TT	TT <CR> - Force REMOTE DIAGNOSIS line from mode 3 to mode 2.	NA
8080 Register Commands		
LR	LR <CR> - Command to set into the 8080 RAM, the I/O register, to be either deposited or examined.	NA
DR	DR <CR> - Command to deposit a number into the last specified 8080 I/O register.	NA
ER	ER <CR> - Command to examine one of the 8080 internal registers and display the contents of that register.	NA

NOTES

1. Lixx - The address consists of a control number and a register address. If the console attempts to access its own register, no response occurs.

CTL	Register Address	Register
0	100000	Memory status register
1, 3	763000-77	UBA paging RAM
1, 3	763100	UBA status register
1, 3	763101	UBA maintenance register
1, 3	7XXXXX	Unibus device register

2. DS - The default value for the RH11 base address is currently the only value permitted. Also, a carriage return in response to any question retains the current value.

```
>>UBA? 1 <CR>
>>RHBASE?, 776700 <CR>
>>UNIT? 0 <CR>
```

3. MS - The default value for the RH11 base address is currently the only value permitted. Also, a carriage return in response to any question retains the current value.

```
>>UBA? 3 <CR>
>>RHBASE? 772440 <CR>
>>TCU? 0 <CR>
>>DENS? 1600 <CR>
>>SLV? 0 <CR>
```


Table 3 Console Error Messages

Message	Meaning
?A/B	A not equal to B. (A and B copies of a microcode field did not match.)
?BC xx	BC command failed. BOOTCHECK error messages are of the form: "?BC WWYYYY" WW=10 Indicates a failure during the CRAM check portion of BOOTCHECK. YYYY will be failing CRAM address. WW=04 Indicates a failure during the memory check. BOOTCHECK is trying to verify page 1 of MOS memory, and tests address 1000-1777 for ability to hold all ones, all zeroes, and to sequence through that page of memory correctly. YYYY will be the failing memory address. WW=00 Indicates a failure during the KS10 bus check. BOOTCHECK is floating a one, then a zero across the KS10 bus. YYYY These are the failing bits in octal. Numbers will range from 0 to 43, which corresponds to decimal 0-35.
?BFO	Buffer overflow. (Too many characters typed; console's 80 character input buffer is full.)
?BN	Bad number. (Character typed is not an octal number.)
?BT xx	BT command failed. 8080 error messages of the type "?BT XXXYYY". These messages can occur anytime the 8080 is trying to access either a disk or tape. A message of the form "?BT XXXYYY" should be interpreted as follows: XXX=001 Means for disk that an error was encountered while trying to read the home blocks. Just about anything can cause this error, including no disk pack in the drive, wrong unit selected, incorrect RH base specified, wrong UBA selected, or bad disk drive. This message also occurs if both the home block and alternate home blocks can be read, but neither has the home block ID ("HOM" in six bit). Means for tape that an error was encountered while trying to read the first page of microcode from the magtape. Anything could be wrong in the CPl1 to magtape path, including wrong unit selected, wrong RH base address, wrong UBA, wrong slave, wrong density, bad tape drive, bad TM02, bad magnetic tape, or tape in the wrong format. This error can occur on any 8080 command or process that accesses disk or tape. XXX=002 Means that a disk error was encountered while trying to read the page of pointers which makes up the 8080 file system. If you get this far, the home blocks may have been read successfully. The problem could be a pack that is not in the format required for 8080 loading, the home blocks are bombed, or bad disk drive or pack. This error can occur on any 8080 command or process that accesses disk or tape.

Table 3 Console Error Messages (Cont)

Message	Meaning
XXX=003	Means that a disk error was encountered while trying to read a page of the microcode. If you get this far, the problem could be a pack not in 8080 format, or bad disk drive or pack. This error can occur on PWR FAIL recovery, SCE soft CRAM error recovery, VD, BT, or MT commands.
XXX-004	Means that the microcode did not successfully start running after a BT, MT, MB, or LB command. This error will always occur when you do an LB, before the system microcode is loaded.
XXX=010	Means that an error was encountered while trying to read in the PRE-BOOT program. Problems could be the same as 003 above. If accessing the tape, failure could have occurred while doing a skip over the microcode file, or in the reading of the PRE-BOOT program itself. Tape could be in the wrong format. This error can occur on LB, MB, or FORCED RELOAD.
YYY	Indicates the lower 8 bits of the 8080 address of the failing "Channel Command List" operation. Do not waste your time looking in the listing, unless you are positive that the RH11 or disk drive is bad. Instead, type EI on the CTY. It will print out the contents of the RH11 register that has the error bits set. That will give you more information than an 8080 listing. If you do find your way through the 8080 listing, you will do an EI anyway, so do the EI first.
?BUS	Bad KS10 bus. (All bus lines not zero after power-up or reset.)
?CCYC	Command/address cycle failed. (KS10 bus data failure detected during DB command; good and bad data printed.)
?CHK xx	PROM checksum error. (Bad checksum for PROM chip xx where xx = 1, 2, 3, or 4.)
?DCYC	Data cycle failed. (KS10 bus data failure detected during DB command; good and bad data printed.)
?DNC	Did not complete. (HA or SM command did not cause microcode to enter halt loop.)
?DNF	Did not finish. (ST, CO, or EX command did not complete.)
?FRC	Forced reload. (Monitor has requested reload; 8080 halts the KS10, reloads the PRE-BOOT program, and starts in KS10 memory location 1000.)

Table 3 Console Error Messages (Cont)

Message	Meaning
?IA	Illegal address. (Address typed is out of range.)
?IL	Illegal command. (Command typed is not valid.)
?IL	Incorrect password. (Password entered via KLINIK line does not match password entered at CTY.)
?KA	Keep-alive error. (During timesharing, the monitor failed to update the keep-alive count for a period of approximately 15 seconds.)
?MRE	Memory refresh error. (Incomplete KS10 MOS memory cycle. Error occurs when memory must be refreshed in hung state.)
?NA	Not available. (Console not enabled to receive KLINIK line input.)
?NBR	No bus response. (Console did not receive GRANT after requesting KS10 Bus.)
?NDA	No data acknowledge. (Console did not receive DATA CYCLE signal after a data request.)
?NR-SCE	Nonrecoverable soft CRAM error. This message is followed by the standard "?PAR ERR" message.
?NXM	Nonexistent memory. (Deposit or examine command referenced nonexistent KS10 MOS memory location.)
?PAR ERR xx	System parity error. (CPU clock stopped due to system parity; xx = contents of the following console status registers in the order indicated: 100, 303, 103)
?PWL	Password length error. (Password longer than six alphanumeric characters.)
?RA	Requires argument. (Command typed requires an argument.)
?RUNNING	Clock running. (Command typed requires CPU clock to be stopped.)
?UI	Unknown interrupt. (Console received interrupt but CTY or KLINIK line has no character.)
%SCE XXXXXX	Soft CRAM error. XXXXXX represents the error address. 8080 is attempting to recover by reloading the CRAM and continuing the instruction that got the parity error.

